TANDY®

Service Manual

25-3500

Tandy® 1400LT LAPTOP COMPUTER

Catalog Number: 25-3500

SPECIFICATIONS

Microprocessor	NEC V-20 (8088 equivalent).
Clock Speed	7.16/4.77 MHz (switchable).
Operating System	Includes MS-DOS/GW-BASIC 3.2
Memory	16K ROM, 768K RAM. 640K accessible by MS-DOS, 128K available for RAM-based disk drive or print spooler.
Keyboard	Full-size, 76 keys.
LED Indicators	Caps Lock, Num Lock, Low Battery, Scroll Lock, Standby Mode.
Display	Backlit "Supertwist" LCD, 640 × 200 pixels, 80 × 25 characters, aspect ratio 1 : 1.4. Optional RGBI Color Monitor.
Disk Drives	Two internal 720K 3.5 inch double-sided, double-density.
Modem	Optional 1200-baud, Hayes-compatible mode.
External Connections	AC Adapter DB-25 Parallel Printer. DB-9 Serial Port. RGBI Color Monitor. Composite Video Out. External Disk Drive. Enhanced Keyboard.
AC Adapter	15 VDC 700mA, UL listed.
Battery	Removeable 12 Volt, 2200 mAh. 4 hours of continuous use.
Other Features	Battery-powered Clock/Calender, Standby Mode and Speaker.
Dimensions	3-1/2 × 14-1/2 × 12-3/8 inches
Weight	13.5 lbs.

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I INTRODUCTION

This manual is prepared for the Tandy 1400LT technicians working in the field or in repair centers.
This manual is divided into Eight sections and six appendices:

Section I

This section provides general information on the Tandy 1400LT such as specifications, external views and internal views.

Section II

This section describes the disassembly and reassembly procedures.

Section III

This section describes the preventive maintenance and adjustment of the Tandy 1400LT.

Section IV

This section describes the general theory of operation for the Tandy 1400LT.

Section V

This section describes how to troubleshoot the Tandy 1400LT.

Section VI

This section provides a parts list and an exploded view of the Tandy 1400LT.

Section VII

This section provides the schematics of the Tandy 1400LT.

Section VIII

This section provides the PCB diagrams and Silkscreen views of the PCBs of the Tandy 1400LT.

Appendix A

This Appendix provides the LCD Specifications.

Appendix B

This Appendix provides the EL Back Light Manual for replacement.

Appendix C

This Appendix provides the 3.5-inch FDD Specifications

Appendix D

This Appendix provides the 3.5-inch FDD maintenance manual.

Appendix E

This Appendix provides the character code table.

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This Appendix provides the description of I/O commands.

I-1 System Overview

The Tandy 1400LT is a fully functional PC compatible.

The Tandy 1400LT represents a remarkable breakthrough in portable computer technology. Its 8088-equivalent microprocessor (NEC-V20) has a 7.16 MHz clock speed (VS. 4.77MHz for other PC-compatible laptops). And the 768K RAM is enough memory to run all of your important applications. The Tandy 1400LT comes with two 720K 3 1/2" built-in disk drives. The Tandy 1400LT features a high-quality backlit liquid crystal display. The 80-character by 25-line resolution. The Tandy 1400LT also includes a parallel printer adapter, an RGB monitor output, composite monitor output, Standby mode, real-time clock and RS-232C serial interface. It also supports an external keyboard and handy, removable battery pack with Low-battery warning.

I-2 External View

1. **Keyboard.** The keyboard features 76 typewriter-keys and Special-Function keys.
2. **LCD Unit.** The Tandy 1400LT display has 25 lines that allow 80 character on each line.
3. **Power Switch.** Push this switch to turn the power ON or OFF.
4. **Display Adjustment Dial.** This control adjusts the contrast of the LCD Display relative to the viewing angle.
5. **NUM, CAPS, Scroll Lock Indicator.** These RED LEDs will illuminate when NUM-Key, CAPS-Key or Scroll Lock-key are held down.
6. **Low Battery Indicator.** Before the Tandy 1400LT's operation batteries become exhausted, this indicator will illuminate.
   (refer to [Page 1-8]: Battery Voltage Warning)
7. **Standby-Mode Indicator.** When nothing is input for about 1~239 minutes (software selectable) after the last keying in the system automatically turns to standby mode. In standby mode system indicates a GREEN LED light.
8. **Boot exchange switch.** When you use an external disk drive, you can change the drive designations. Use this switch with the boot select switch set to INT, the drives are designated as follows.
   Left Drive..... Drive A
   Right Drive..... Drive B
   External Drive ..... Drive C

   with the boot select switch set to EXT, the drives are designated as follows.
   Left Drive..... Drive C
   Right Drive..... Drive B
   External Drive ..... Drive A
9. **External Power Adapter Connector.** Connect the appropriate end of AC Power Adapter.
10. **Monitor (LCD/CRT) Selector.** This selector allows you to select either a internal LCD or external CRT. When you start the system with the monitor switch in the OFF position, the default display is LCD. Set the switch to ON before turning on the system to use a CRT as the default display.
11. **Printer Connector.** For hard-copy printouts of information, attach parallel printer to this connector, using a printer cable.
12. **RGB Connector.** To use an RGB direct-drive color monitor, connect its cable to this connector.
13. **Video Connector.** To use a composite CRT monitor, connect the cable to the connector.
14. **RS-232C Connector.** Attach a DB-25 cable to this connector when you need to receive or transmit serial information.
15. **External disk Drive connector.** To use an optional external floppy disk drive, connect the cable to the connector.
16. **External keyboard Connector.** To use a Tandy Enhanced keyboard (cat. No. 25-4038) or an IBM PC-compatible keyboard, connect the cable to the connector. And select EXT during Setup mode. If you are using a Tandy Enhanced keyboard, it must be set to IBM XT compatible mode.

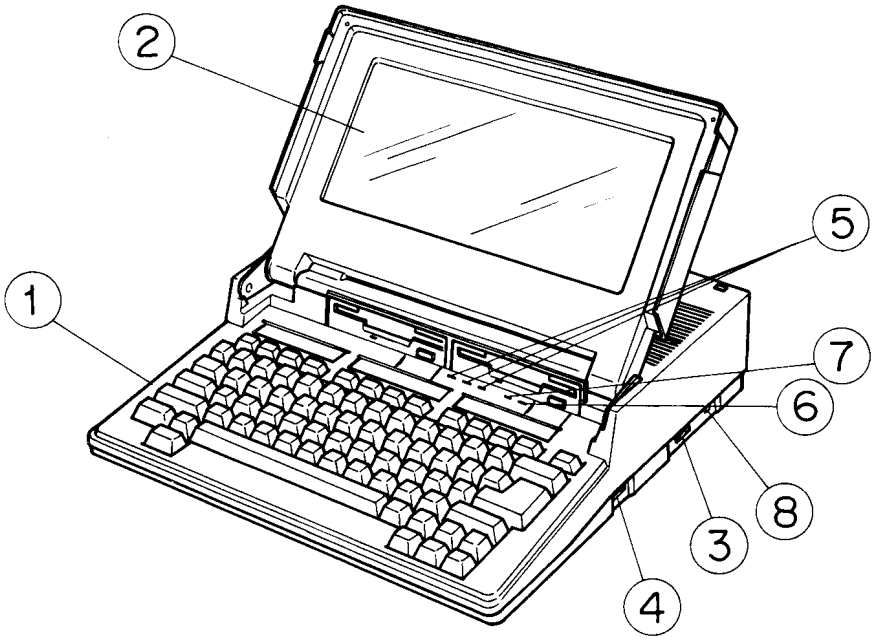


Figure 1-1. Front View

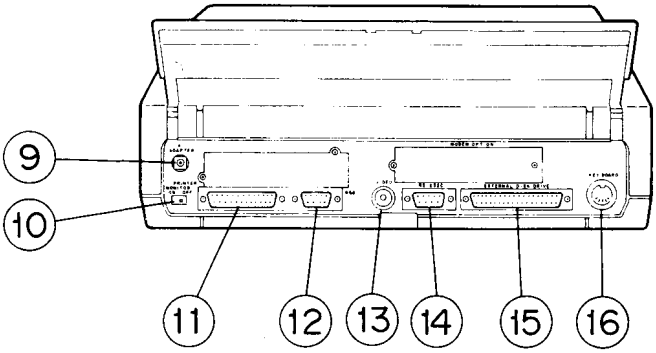


Figure 1-2. Rear View

I-3 Internal View

The Tandy 1400LT Consists of eight printed circuit boards:

- LCD PCB
- Keyboard PCB
- Main PCB
- Memory PCB
- Power PCB
- SUB PCB
- LED PCB
- FDD PCB

[Main electrical components will be shown in these figures]

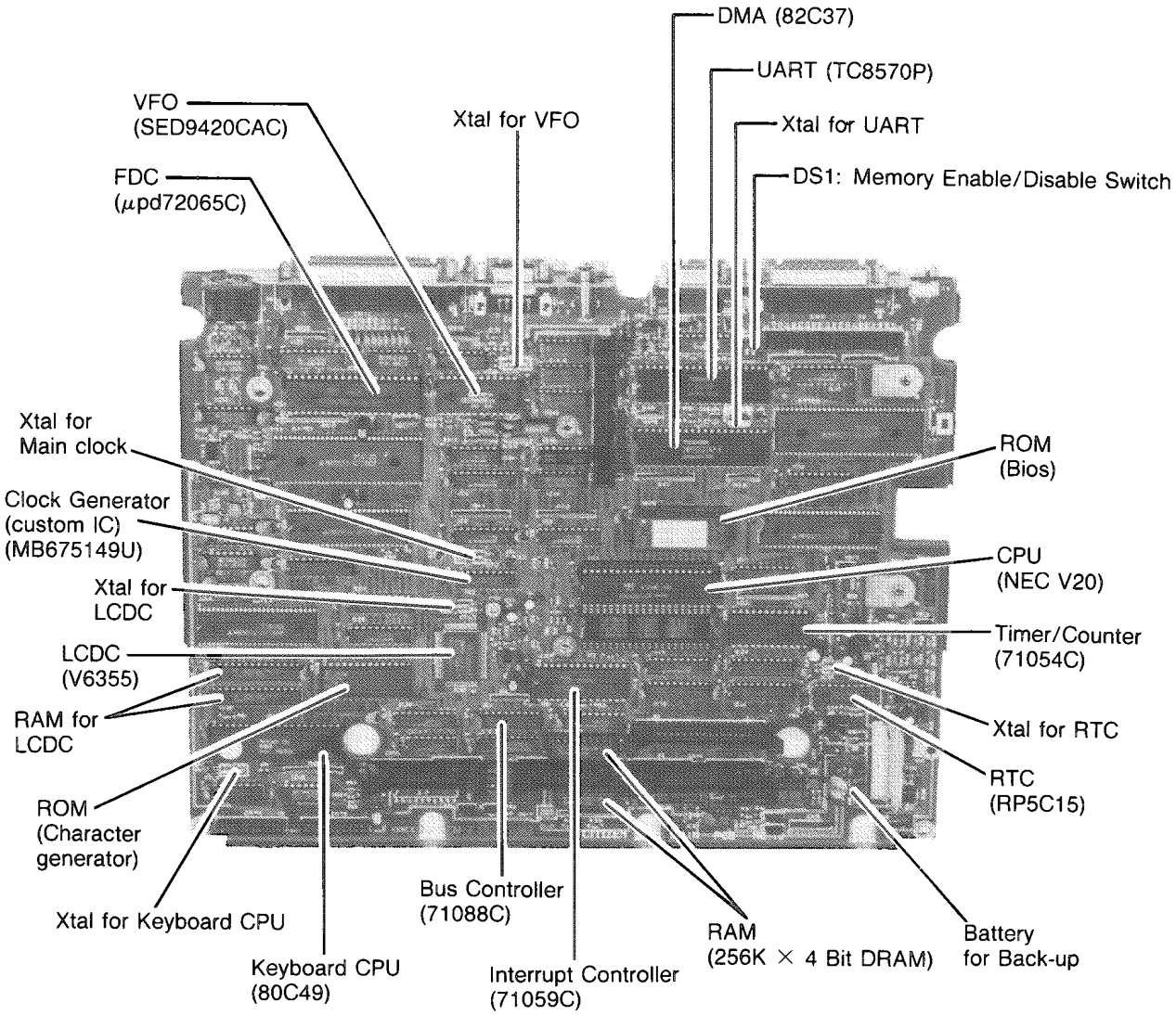


Figure 1-3. Main PCB

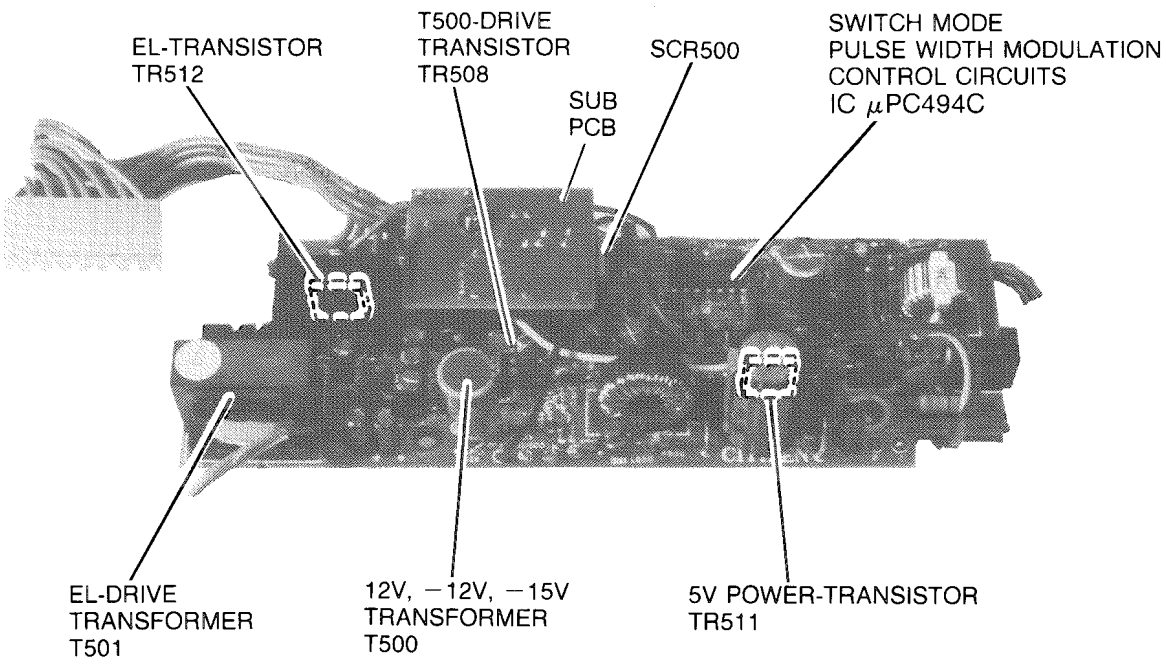


Figure 1-4. Power PCB

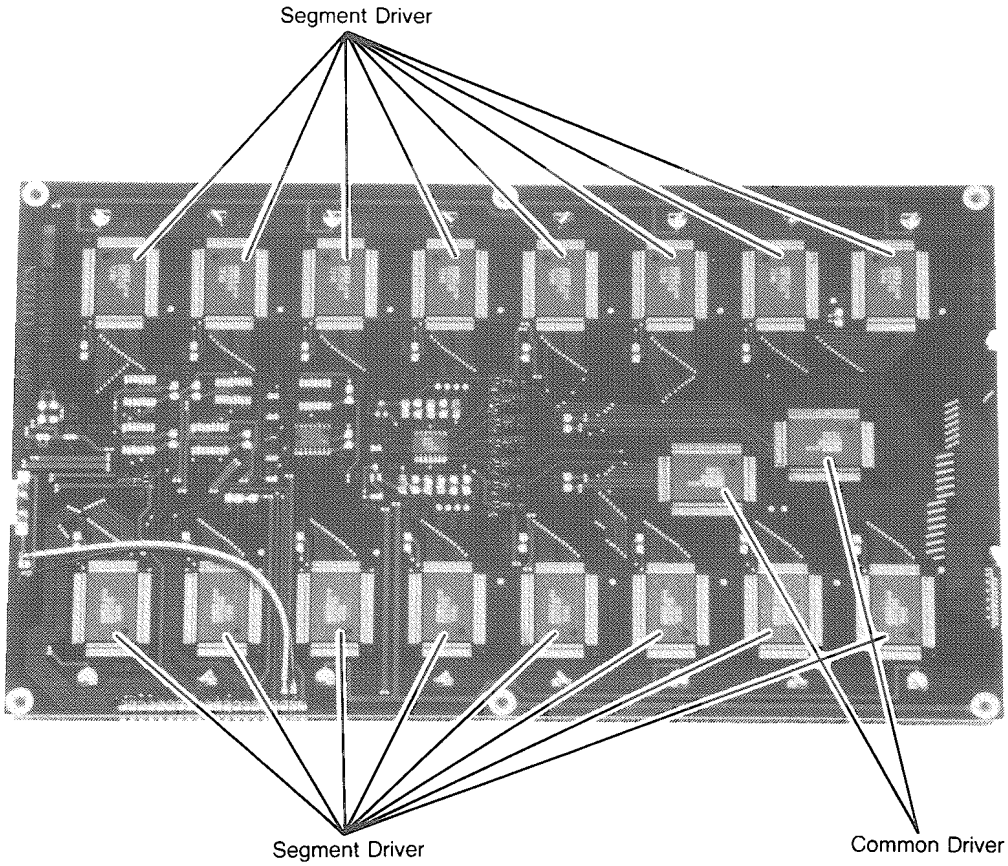


Figure 1-5. LCD PCB

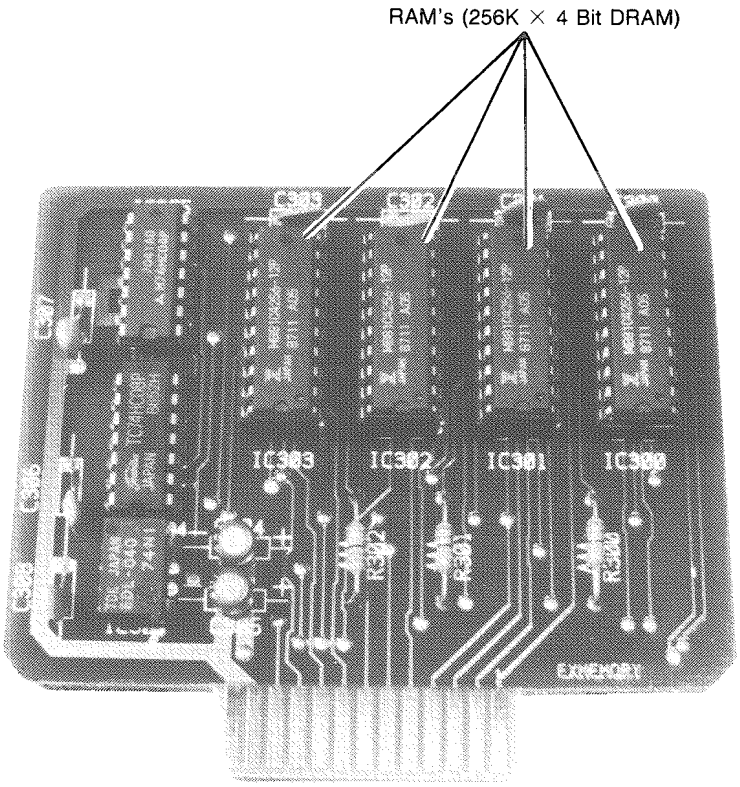


Figure 1-6. Memory PCB

I-4 Hardware Specifications

CPU	NEC V20 (μPD70108)
CPU CLOCK	4.77/7.16 MHz selectable.
RAM	
Capacity	768Kbyte
Device	1Mbit type DRAM (256Kbit by 4) 40000H - 9FFFFH and DC000H - FBFFFH addresses are selectable, enable and disable with DIP Switches. All memory data is lost when the Main Power is OFF.
ROM	Minimum 16Kbyte
DISPLAY	
Control Device	V6355 LCD Controller
Graphic Resolution	640 * 200 dots.
Character Display	80 Characters × 25 lines (or 40 Characters × 25 lines)
Display Devices	Following devices can be used 1. Super twist nematic LCD panel with EL back light. 2. CRT with IRGB input. 3. CRT with NTSC not color COMPOSITE input
Display Control	Basically conforms to IBM-CGA
Video RAM	16Kbyte (64Kbit type SRAM × 2)
Character Generator	Character ROM is used for the character display mode.
Base System Display Device	Consists of STN LCD panel with EL back light. (640*200 dots). The time sharing gradation system enables 8 gradation displays. In addition, the display can be switched to the CRT by software and or monitor switch. (IRGB CRT and or NTSC Composite CRT)
Effective Display Area	9.45″ × 4.13″ (239.96mm × 104.95mm) Dot size - 0.335mm × 0.475mm Dot pitch - 0.375mm × 0.525mm Aspect -1 : 1.4
KEYBOARD	
Number of Keys	76 keys(8 × 10 key matrix)
FDD	
Floppy Disk Driver	OPDB-12A (CITIZEN) Double-Side Double-Density 3.5-inch FDD. Front loading.
Number of Tracks	80
Dimensions	4″ × 5.9″ × 1″ (101.6mm × 150mm × 25.4mm)
Weight	About 1lb. (450g)
Operating Voltage	4.4 - 6.0V
Power Consumption	Read(Write) - 1.8W Typical Stand by - 32.5mW Typical Seek - 6.5W Typical
Rotating Speed	300 RPM
Encoding Method	MFM
Capacity	Unformatted - 1000Kbyte Formatted per disk - 655.4Kbyte (16 Sector/Track) - 737.2Kbyte (9 Sector/Track) - 819.2Kbyte (5 Sector/Track)

Floppy Disk Controller	μPD72065C CMOS type of 765.
Power Supply	Power supply is controlled by software.
No. of Connectable Disks	Controller can control up to 3 FDD. However, to connect the external FDD, an extra power supply is required.
Data Transmission	DMA transmit
Transfer Rate	250Kbit/sec
BOOT Select Switch	Drive assignment depends on the position of the BOOT Select Switch as follows.

	3.5 inch boot	5 inch boot
DRIVE 1	DRIVE A	DRIVE C
DRIVE 2	DRIVE B	DRIVE B
EXT FDD	DRIVE C	DRIVE A

RS-232C INTERFACE

Standard	Conform to EIA Standard
Device	TC8570P DS14C88 and DS14C89AN
Word Length	5,6,7,or 8 bits
Parity	Even, Odd, or None
Stop Bit Length	1, 1.5 or 2 bits
Baud Rate	50,75,110,150,300,600,1200,2400,4800,or 9600BPS
Output Signal Level	Output signal based on +12V and -12V
Input Signal Voltage	SPACE = +3V ~ +15V MARK = −3V ~ −15V

PRINTER INTERFACE

Control	The printer is controlled by the STROBE and BUSY signals. When the printer is not busy, the CPU receives an interrupt signal, IRQ7.
Output	Normal commercial printers can be used, if they have TTL input. When a printer is used, the connector can be plugged in or removed without destroying the inner circuits of the devices regardless of power ON/OFF. In addition, the interface circuits can effectively withstand static charge breakdown.

RTC (REAL TIME CLOCK)

Device	RICHO RP5C15
X'TAL Oscillation	32.768kHz
Battery Back Up	Time counting function is maintained by the battery even when the system is turned OFF.
Accuracy	± 5 minutes/month

POWER SOURCE

Main Battery	12V, 2200mAh , Nickel-Cadmium battery
Back up Battery	A Nickel-Cadmium battery of 3.6V 50mA is used to hold the Time Data of RTC
Battery Voltage Warning	The first warning is indicated by Low Battery RED LED and beep 2 times. The user is instructed to charge the battery voltage to 11.7V ~ 11.9V. After the first warning, the system can be used for about 30 minuites with the FDD 10% duty. The second warning is indicated by Low Battery RED LED flashing and beep 5 times. The user is instructed to shut down the system at a battery voltage of 10.8V ~ 11.4V. User should close current task file. If used after Low Battery warning, the system shuts down and loses all RAM data.

POWER SAVE MODE

When nothing is input for about 1 ~ 239 minutes (software selectable) after the last keying in, the system automatically turns to standby mode. Pressing any key will bring the computer out of STAND-BY MODE. The program being used when STAND-BY MODE is engaged is maintained intact.

NOTE 1: The time of auto standby mode can be set from 1 minute to 3 hours 59 minutes in set up mode.

NOTE 2: In standby mode, system indicates a GREEN LED light.

NOTE 3: In standby mode, memory contents will be maintained by main battery over 11 hours, at the condition of full charge, When main battery is discharged, memory contents are lost. RED LED of Low Battery warning is displayed in standby mode too.

NOTE 4: Input Power rating (AC adapter) voltage 8 ~ 20V (15V, 700mA center ground)

NOTE5: Current consumption (TYPICAL DATA)

	CRT	LCD
Normal use mode	240mA	470mA
FDD SEEK	430mA	700mA
FDD MOTOR ON	350mA	570mA
STANDBY MODE	160mA	

II. DISASSEMBLY INSTRUCTIONS

II-1. Top Case

(1) Turn over the unit and remove the eight screws indicated by the arrows on the bottom face. (Figure 2-1)
NOTE: Turn off the Power Switch when disassembling.

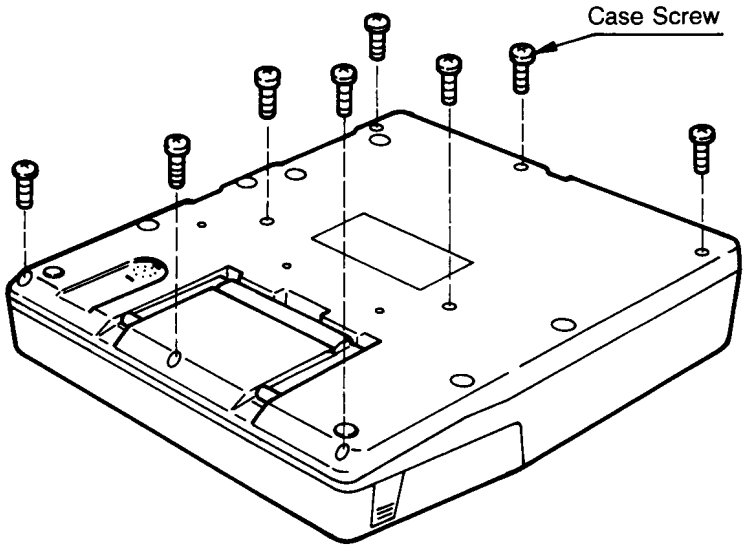


Figure 2-1. Case Screw Removal

(2) Turn over the unit to the normal position and lift the Top Cover (LCD).
(3) Peel off two screw seals on both sides and remove the screws. (Figure 2-2)
(4) Push the ends of the Threaded Bushings with a pointed tool to let them disengage with the Levers.

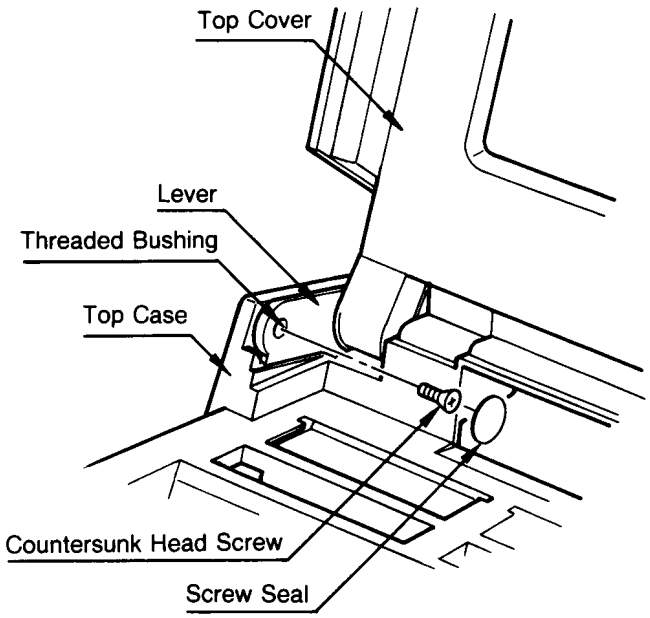


Figure 2-2. Lever Disengagement

(5) Lift off the Top Case assembly from the Buttom Case, pressing the Eject Buttons of FDD's so that they do not catch the Top Case. (Figure 2-3)

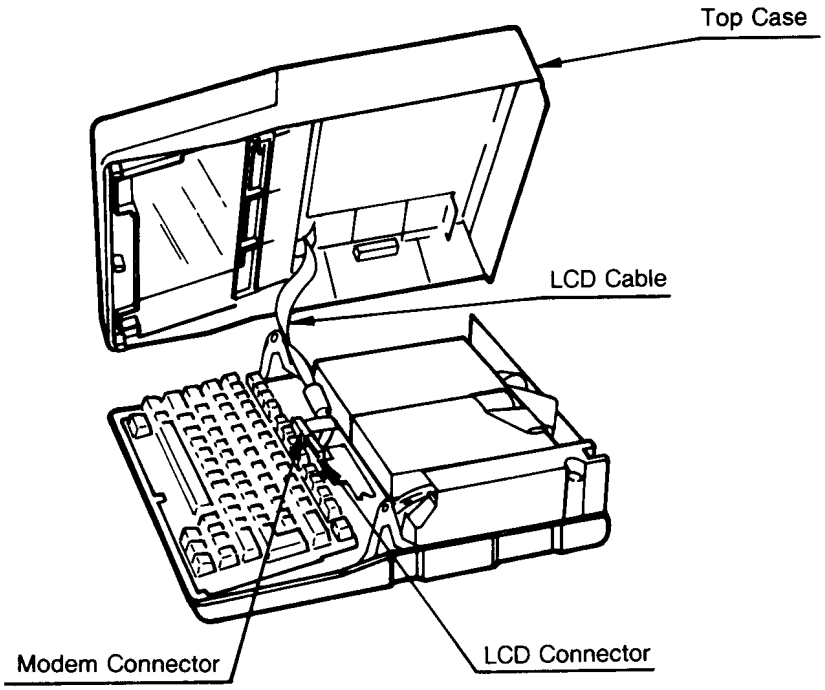


Figure 2-3. Top Case Removal

(6) Pull the claws of the Modem connector in the directions of arrows and remove the Modem Cable. (Figure 2-4)
(7) Remove the LCD connector in the same way as above.
NOTE: The LCD Cable passes behind the Modem Cable.

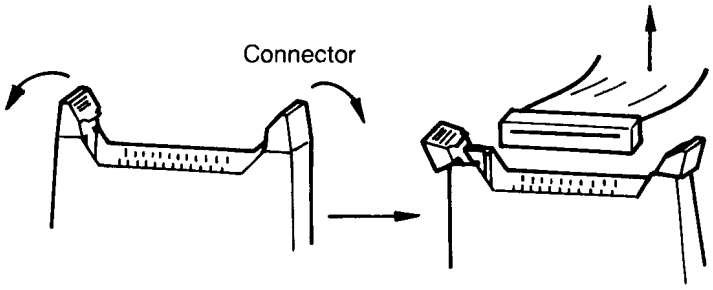


Figure 2-4. Cable Removal

II-2. Battery Cover and Rear Cover

(1) Remove the Battery Cover and the Rear Cover as shown in Figure 2-5. (Push the recessed portion of the Battery Cover to let it disengage with the Top Cover and slide it outward.)

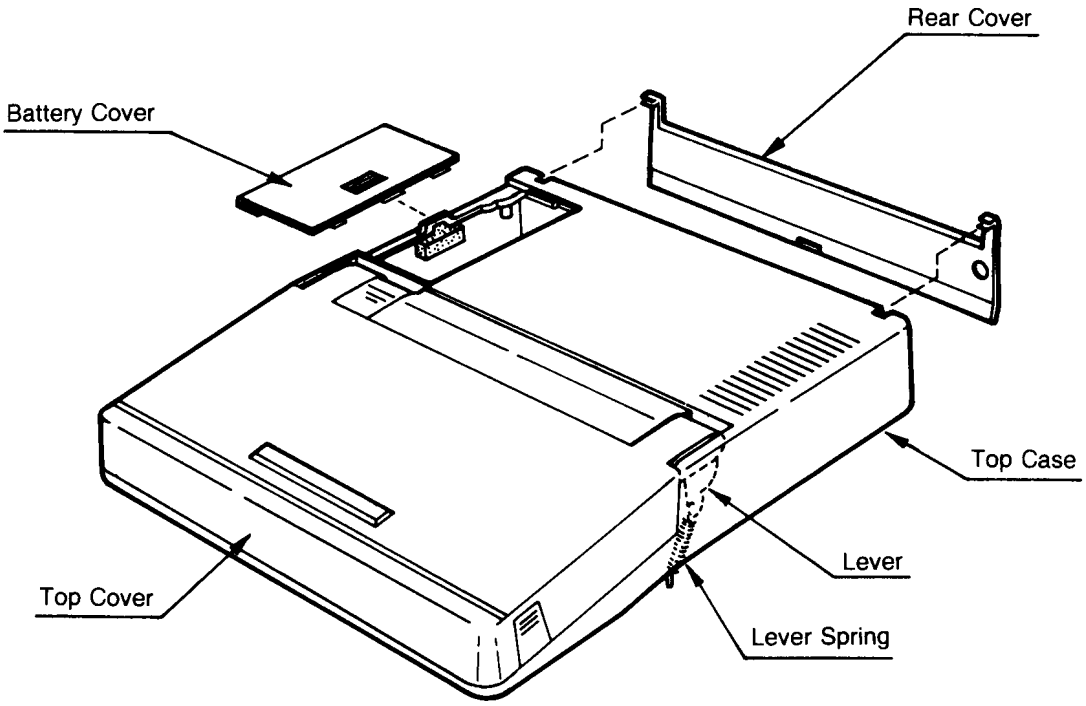


Figure 2-5. Battery Cover and Rear Cover Removal

II-3. LCD Frame, Buttons and LCD

(1) Turn over the Top Case assembly and remove two Lever Springs on both sides. (Figure 2-6)

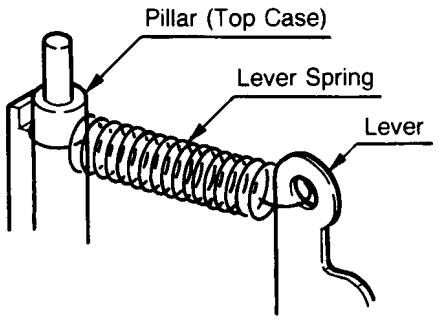


Figure 2-6. Lever Spring Removal

(2) Remove the Top Cover (LCD) from the Top Case. (Figure 2-7)

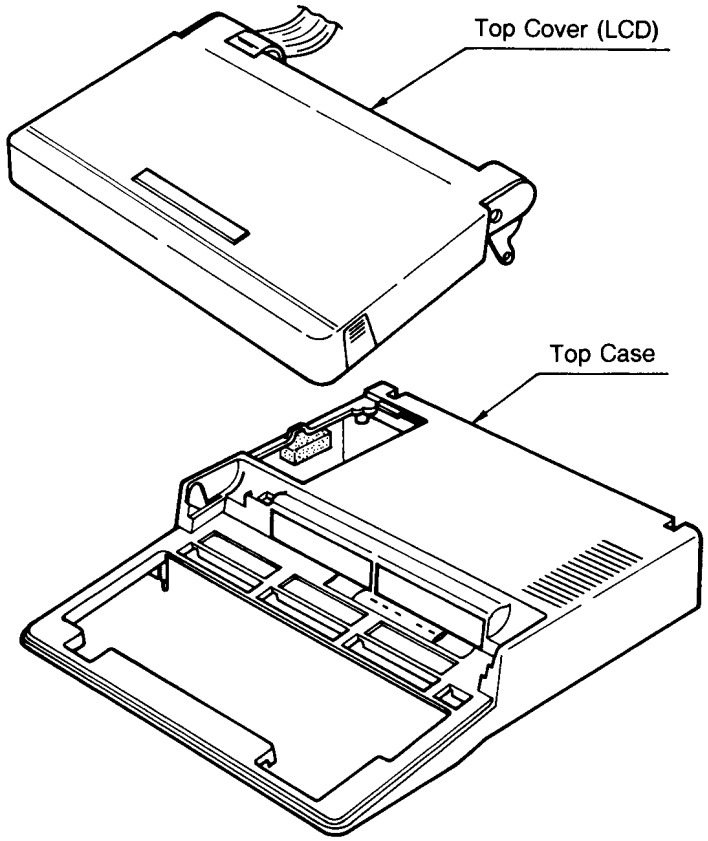


Figure 2-7. Top Cover Removal

(3) Turn over the Top Cover and remove two LCD Frame screws on both sides. (Figure 2-8)
(4) Remove the LCD Frame, then remove two Lock Buttons and two Lock Button Springs on both sides.

(5) Remove the Yoke screws (three at the left, two at the right) and remove the Yokes.

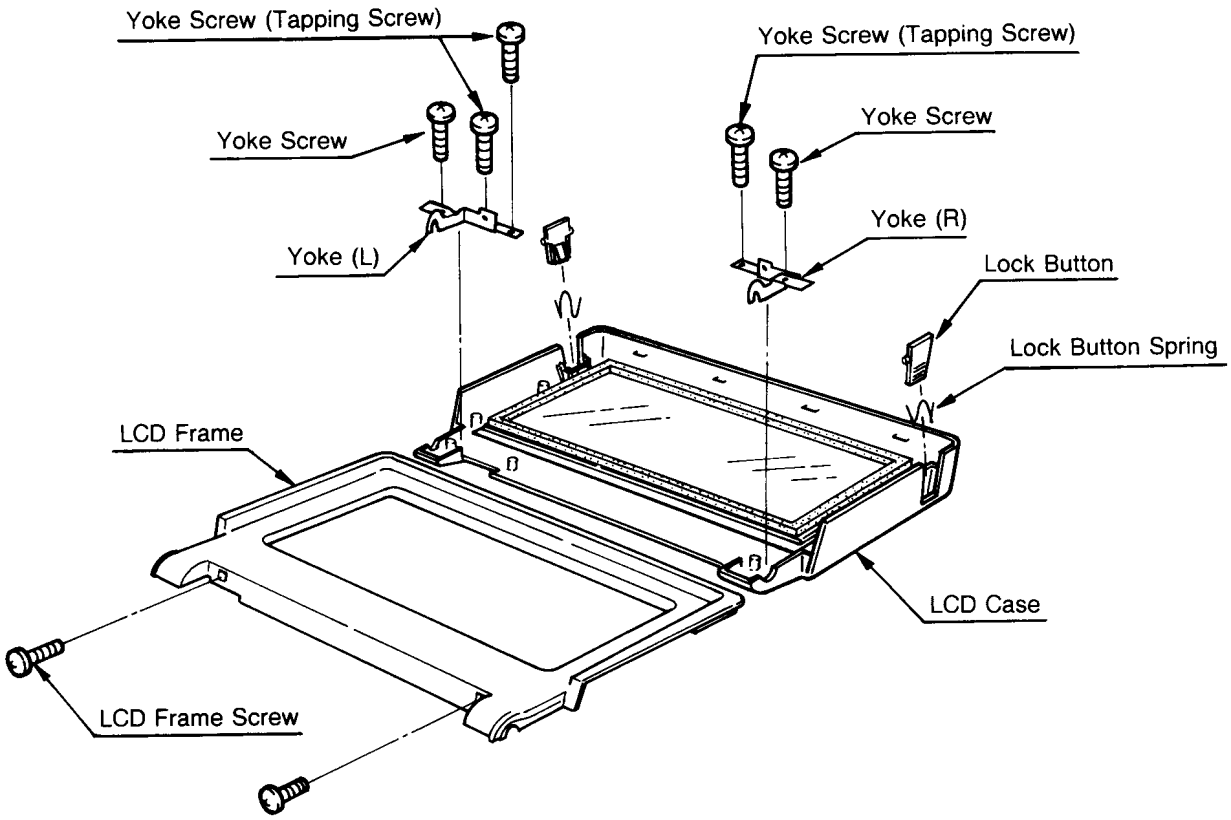


Figure 2-8. Exploded View of LCD Assembly

(6) Remove the Cable Cover from the Cable. (Figure 2-9)
(7) Remove four LCD screws and remove the LCD unit and the cushion below.
NOTE: Be careful not to scratch the display surface of the LCD unit.

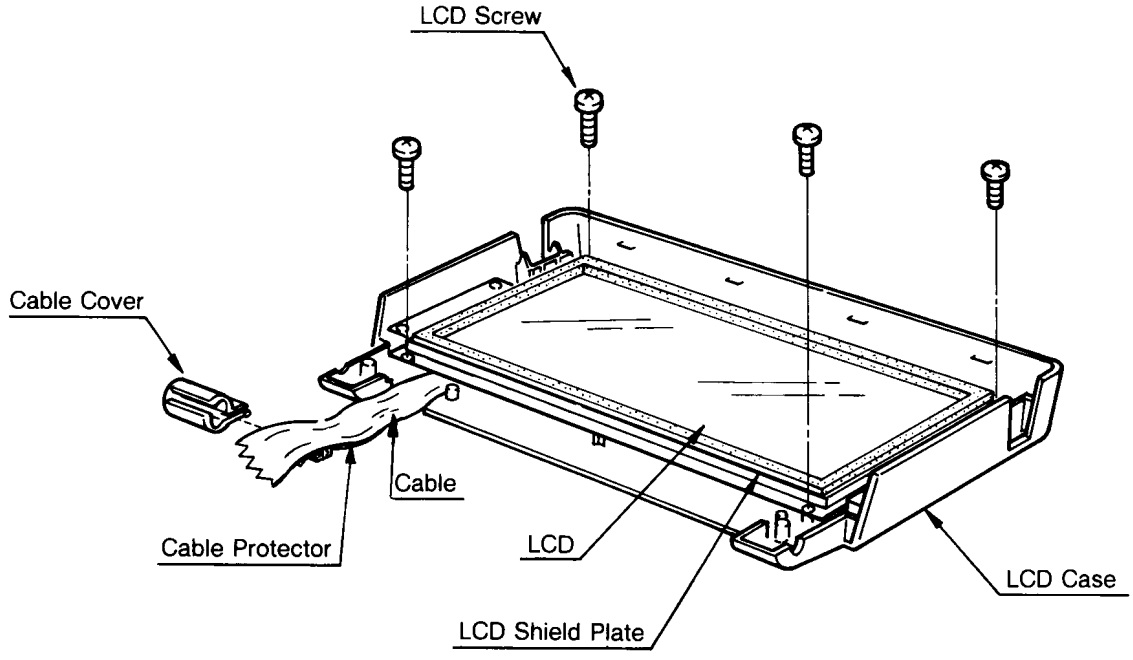


Figure 2-9. Cable Cover and LCD Removal

(8) Remove four Arm screws (two for each) and remove the Arm assemblies. (Figure 2-10)
(9) Pull off the Lever Covers (right and left) from the Arm assemblies.

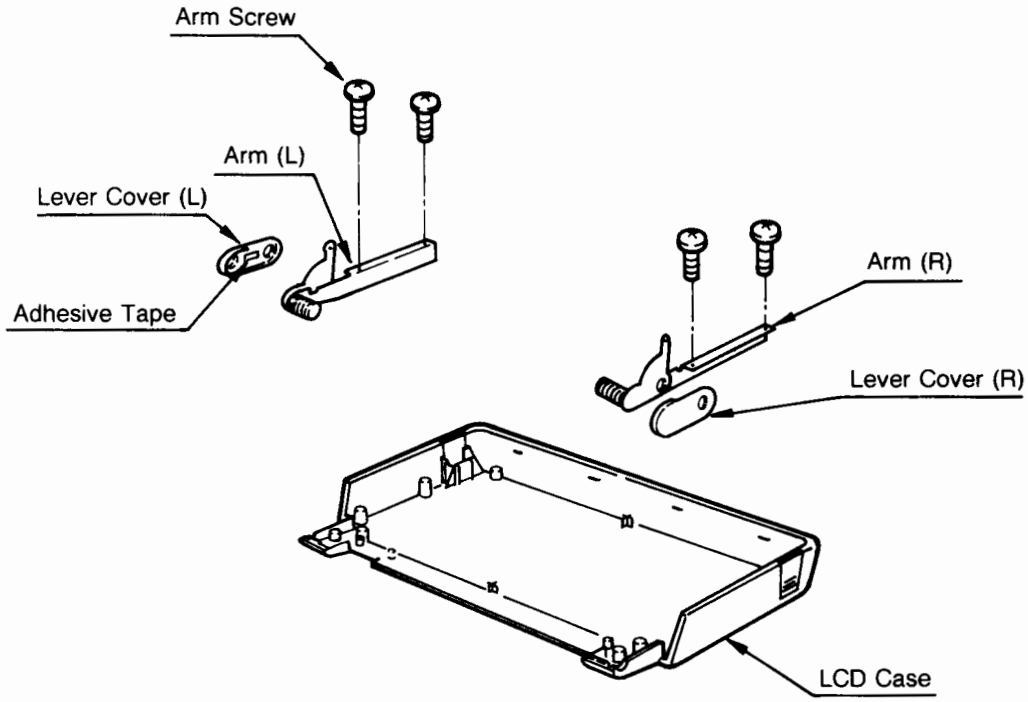


Figure 2-10. Arm Assembly Removal

II-4. LED PCB and Keyboard

(1) Remove four Keyboard screws. (Figure 2-11)
(2) Remove the LED Bracket screw.
(3) Remove the LED connector from the Main PCB and remove the LED unit.
(4) Remove two Keyboard connectors from the Main PCB and remove the keyboard.

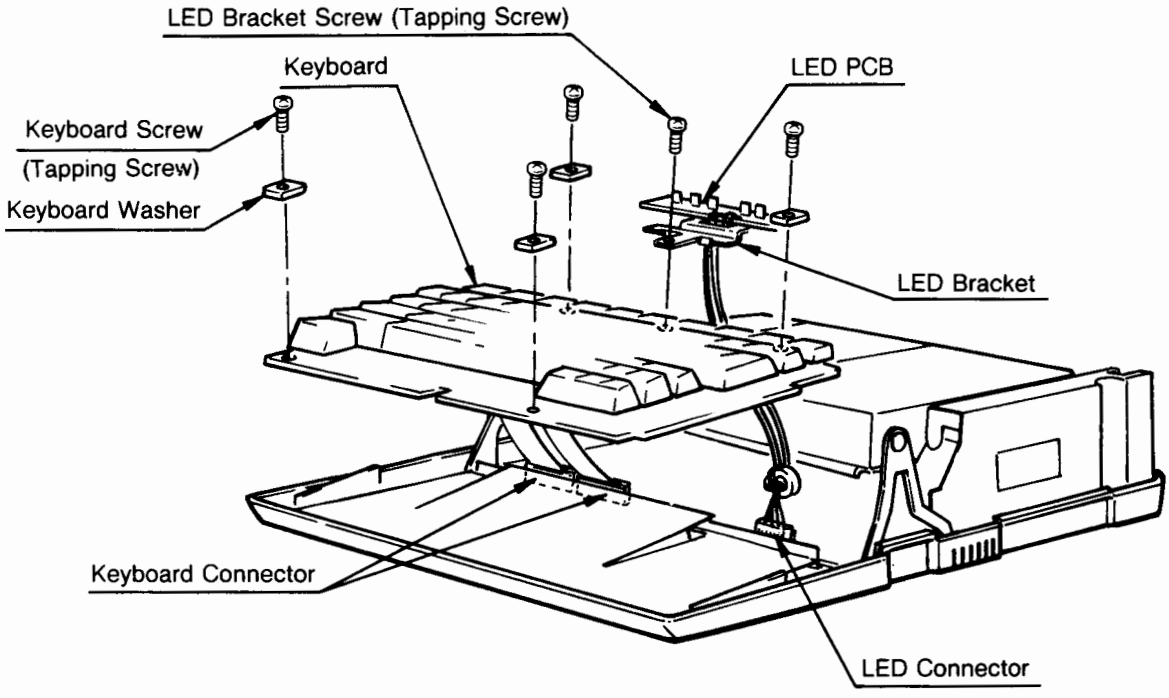


Figure 2-11. LEC PCB and Keyboard Removal

II-5. Battery Pack

(1) Disconnect the Battery connectors and remove the Battery Pack. (Figure 2-12)
NOTE: Be careful not to short-circuit the terminals or wires of the Battery Pack.

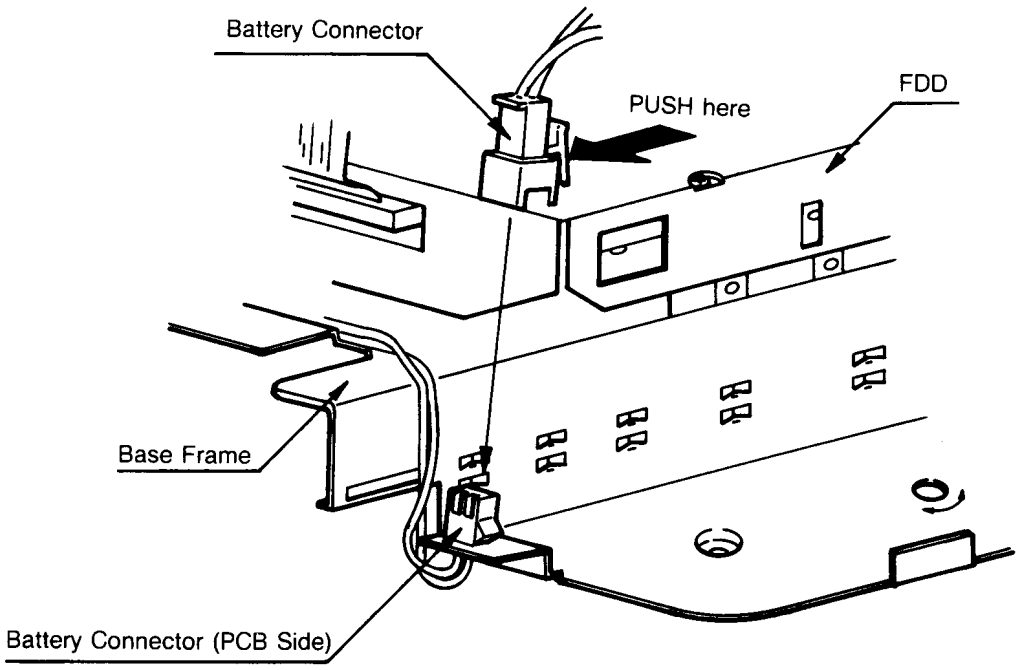


Figure 2-12. Battery connector Removal

II-6. Base Frame

(1) Turn over the Bottom Case, peel off two screw seals with tweezers and remove two Base Frame screws. (Figure 2-13)

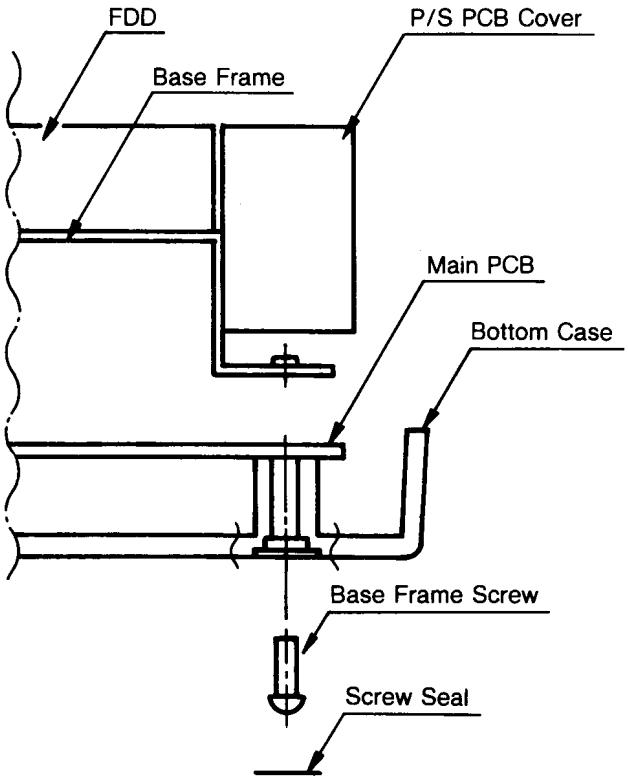


Figure 2-13. Right Side of Base Frame

(2) Turn over the Bottom Case to the normal position and remove two Base Frame screws. (Figure 2-14)

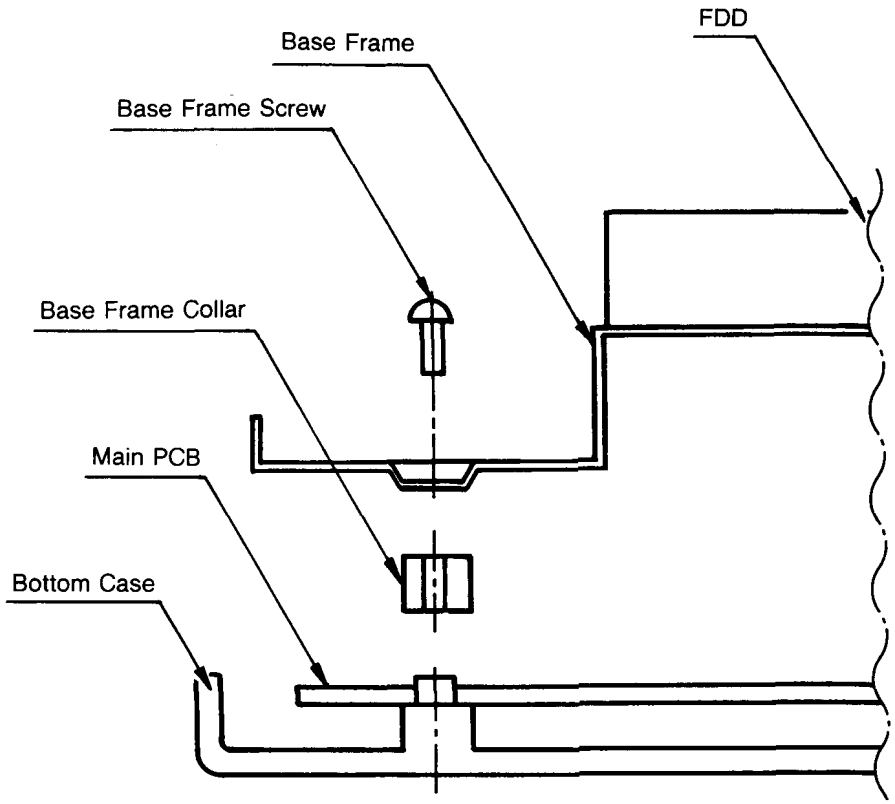


Figure 2-14. Left side of Base Frame

(3) Remove the adhesive tape attaching the Power Switch cords onto the Power Source PCB Cover.
(4) Remove two FDD cable connectors from the rear of FDD's.
(5) Remove the following five connectors from the Main PCB in turn. (Figures 2-4, 2-15)

1. POWER SUPPLY
2. MEMORY
3. EXPANSION BUS
4. EL
5. FDD (Lifting the Base Frame from the Bottom Case.)

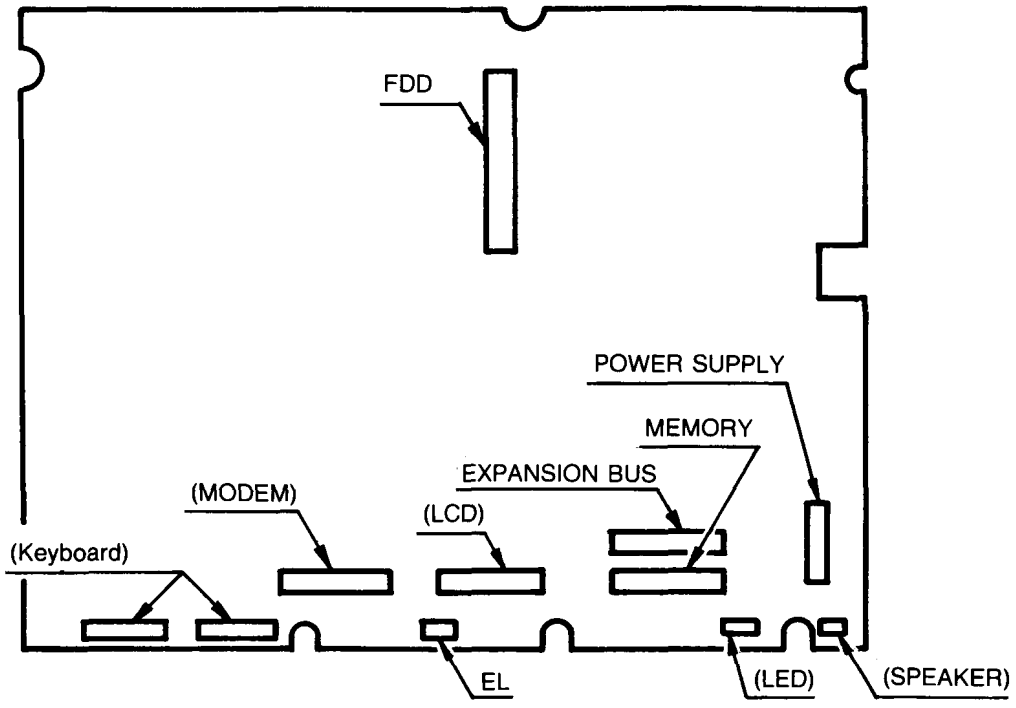


Figure 2-15. Connector Locations

(6) Lift the Base Frame and remove the Power Switch cord receptacles from the terminal pins on the Power source PCB, then take the Base Frame with FDD's out of the bottom Case. (Figure 2-16)

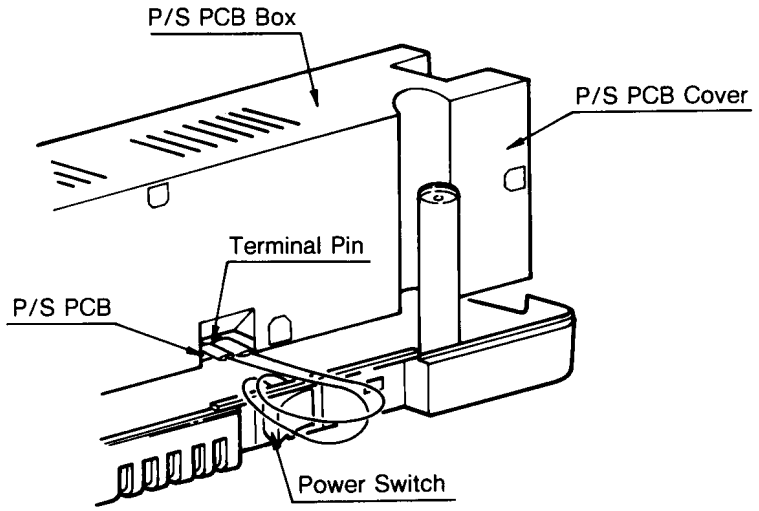


Figure 2-16. Power Switch cord Removal

II-7. FDD

(1) Turn over the Base Frame with FDD's and remove six FDD screws. (Figure 2-17)

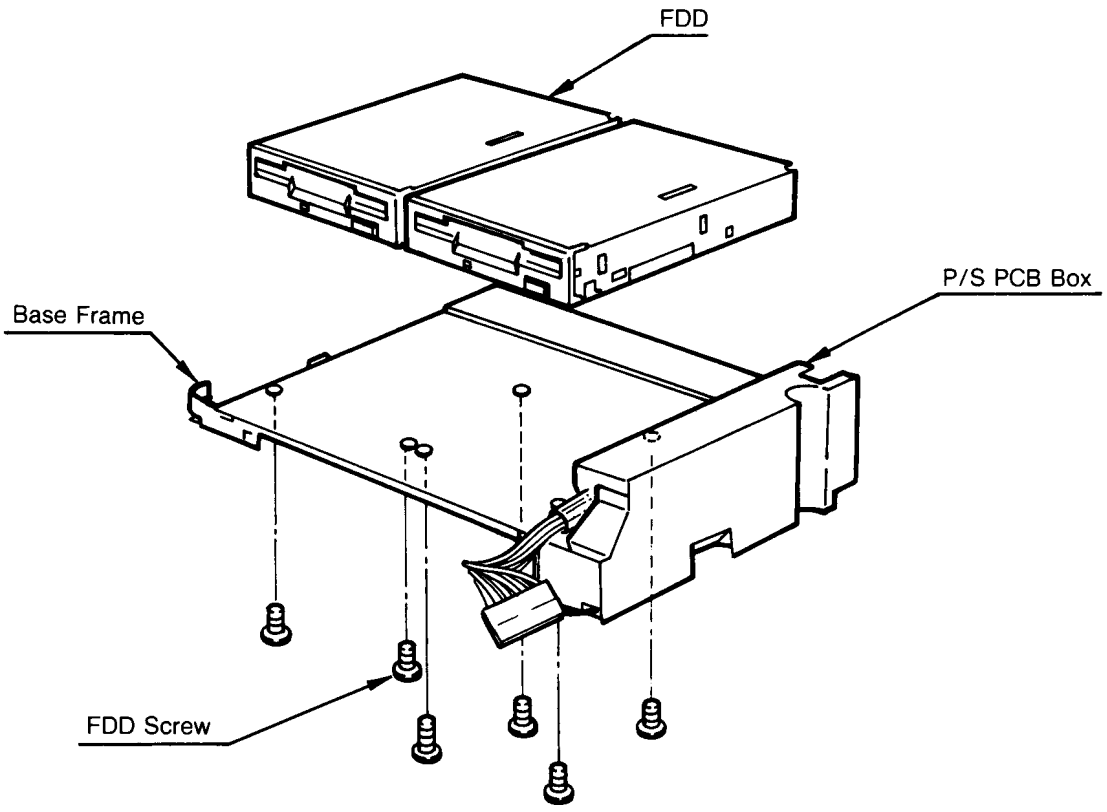


Figure 2-17. FDD Removal

II-8. Power Source PCB, Power Source PCB Cover and Power Source PCB Box

(1) Raise four tabs of the Power Source PCB Box, then remove the Power Source PCB Cover and four cushions. (Figure 2-18)
(2) Remove the Sub PCB screw and remove the Sub PCB.
(3) Remove the Sub PCB Pillar with a nutdriver.
(4) Remove three Power Source PCB screws and remove the Power Source PCB.
(5) Remove four Power Source PCB Pillars with a nutdriver and remove the Power Source PCB Box.

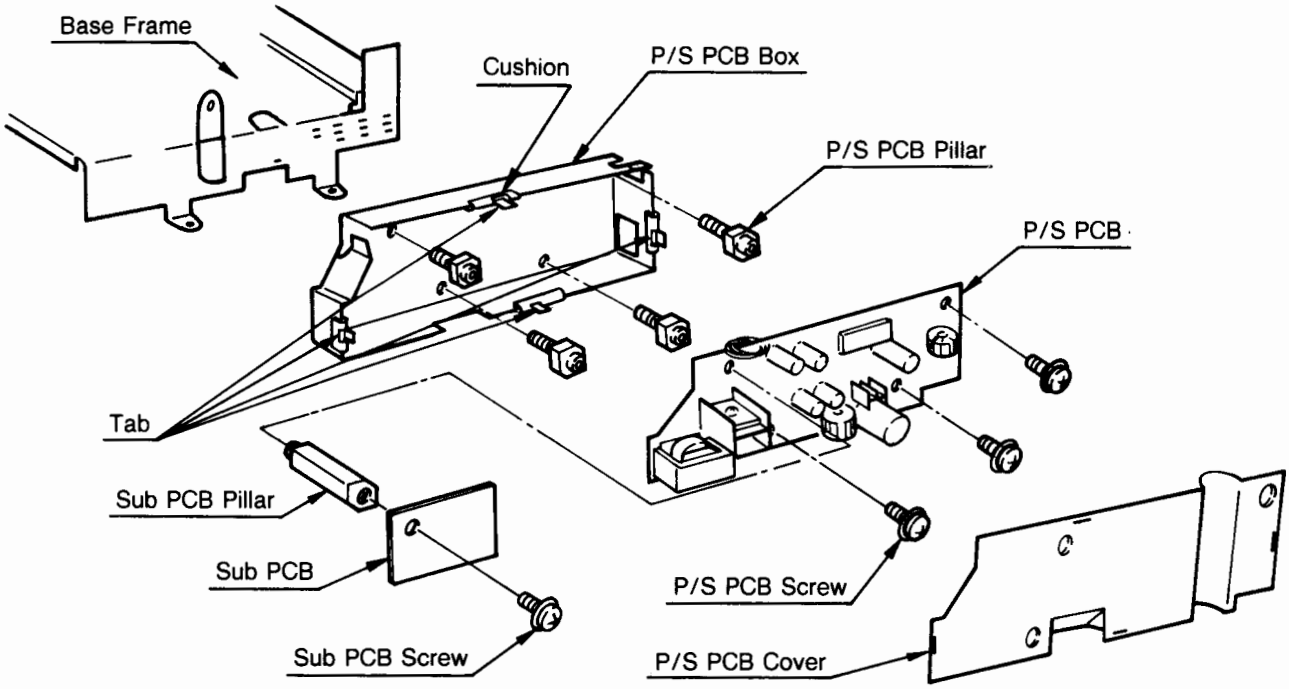


Figure 2-18. Exploded View of Power Source Assembly

II-9. FDD Cable, Expansion Bus Cable, Modem Cable and Memory Cable

(1) Turn over the Base Frame and remove the Memory Spacer and the Memory PCB. (Figure 2-19)
(2) Remove the Expansion Bus Cable and the FDD Cable.
(3) Remove two Modem connector screws and two Memory connector screws, then remove the cables from the Base Frame.

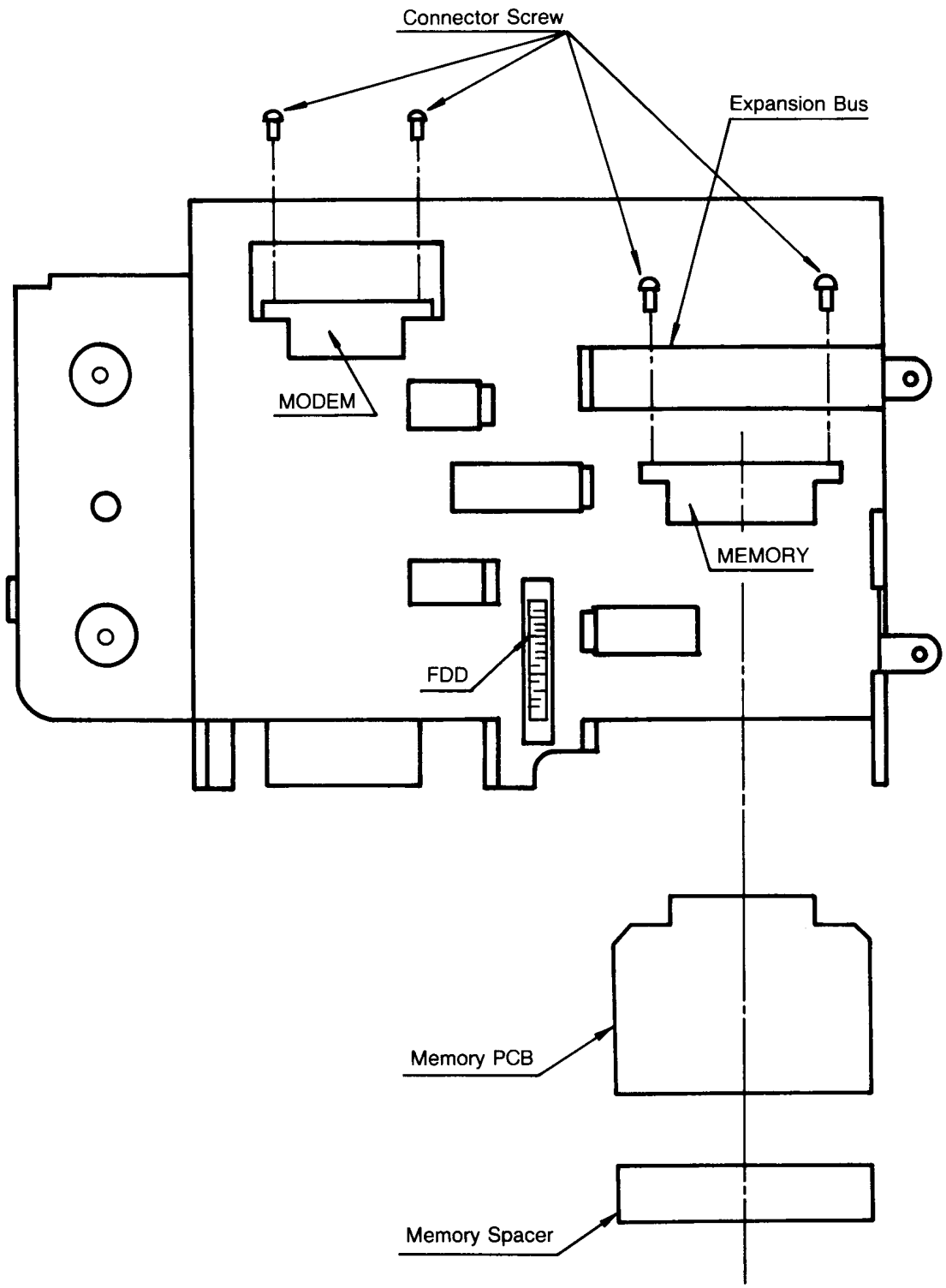


Figure 2-19. Bottom View of Base Frame

II-10. Contrast Knob

(1) Remove the Contrast Knob screw and remove the Contrast Knob. (Figure 2-20)

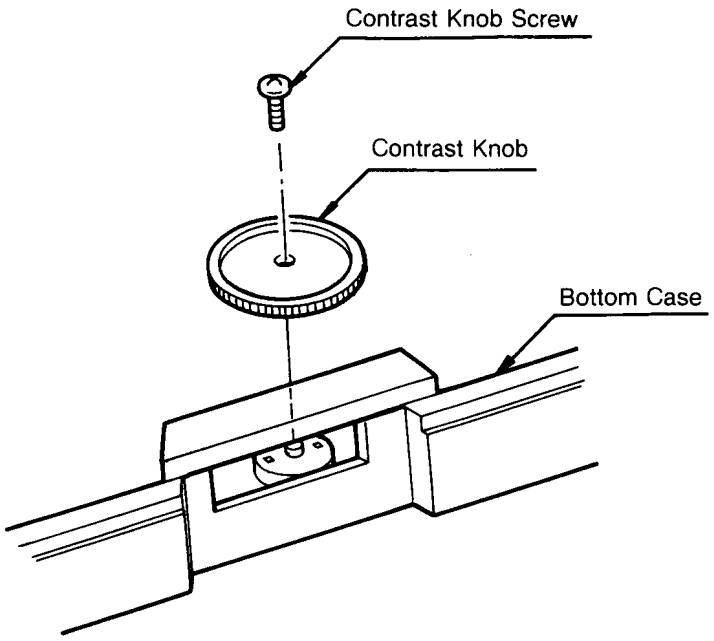


Figure 2-20. Contrast Knob Removal

II-11. Speaker

(1) Remove the Speaker connector from the Main PCB.
(2) Remove the hooked speaker from the Bottom Case. (Figure 2-21)

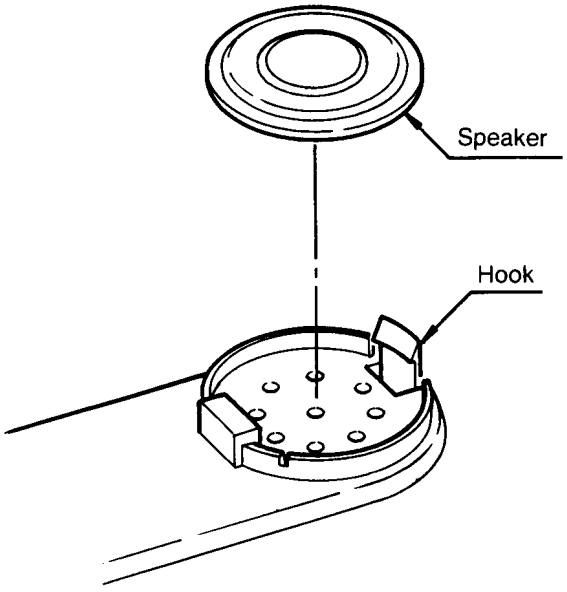


Figure 2-21. Speaker Removal

II-12. Main PCB, Keyboard Shield Plate, Rear Panel and Rear Panel Cover

(1) Remove two connector screws fixing the D-Shell Connectors. (Figure 2-22)
(2) Remove four Main PCB screws.
(3) Remove the Keyboard Shield Plate.
(4) Remove two Conductive Tapes connecting the PCB Shield Plate and the Pedestals (right and left), then take the Main PCB together with the Main PCB Shield Plate and the Rear panel out of the Bottom Case.
(5) Remove three Rear Panel screws and remove the Rear Panel.
(6) Remove eight screws fixing the Main PCB Shield Plate to the D-Shell connectors with a 5 mm nutdriver and remove the Main PCB Shield Plate from the Main PCB.
(7) Loosen four screws fixing the Rear Panel Covers (two for each) and remove the Rear Panel Covers.

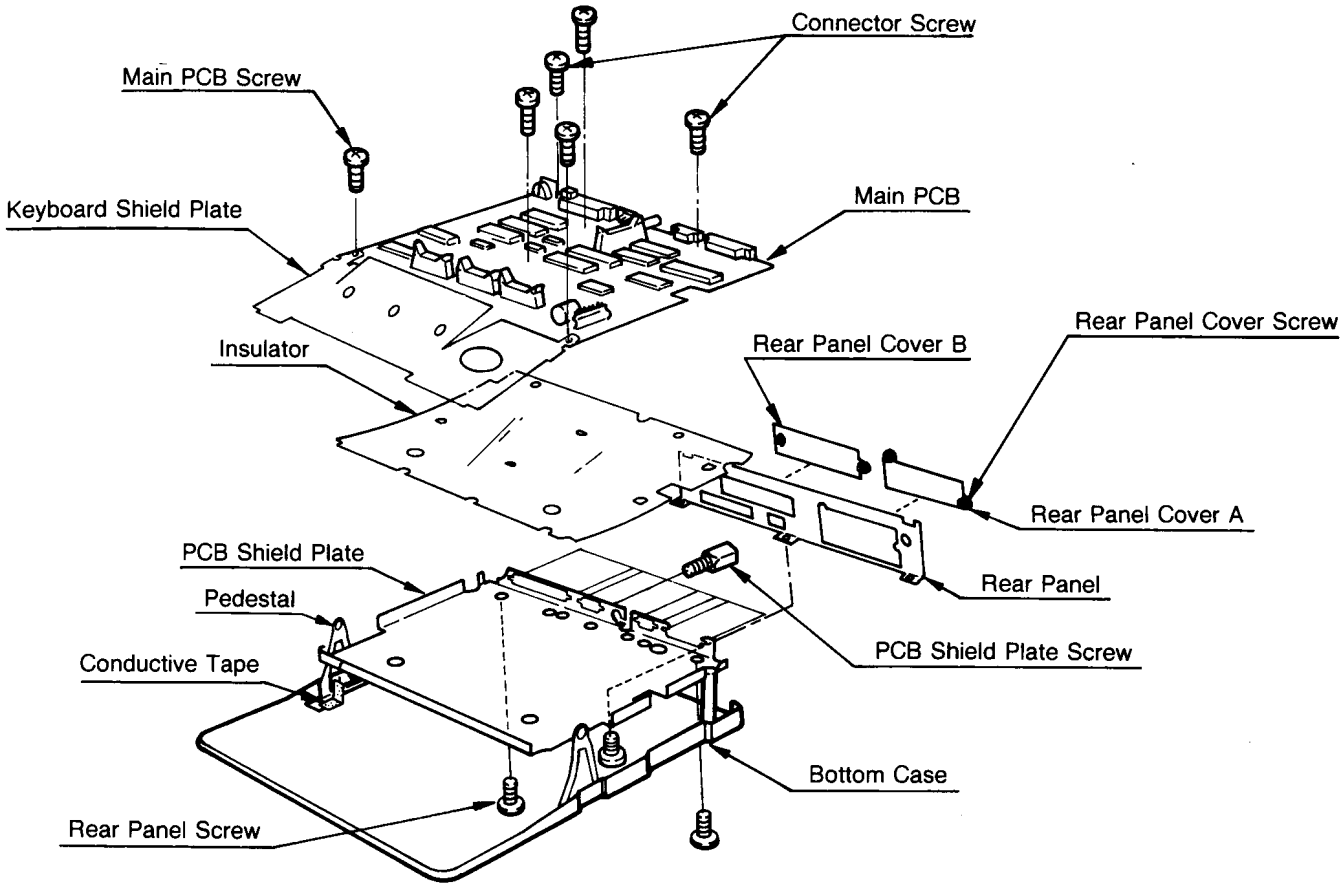


Figure 2-22. Exploded View of Main PCB Assembly

II-13. Pedestals, Handle and Bottom Case

(1) Turn over the Bottom Case and remove four screw Seals with tweezers. (Figure 2-23)
(2) Remove four Pedestal screws and remove the Pedestals.
(3) Pull off the Handle Pins with pliers and remove the Handle.

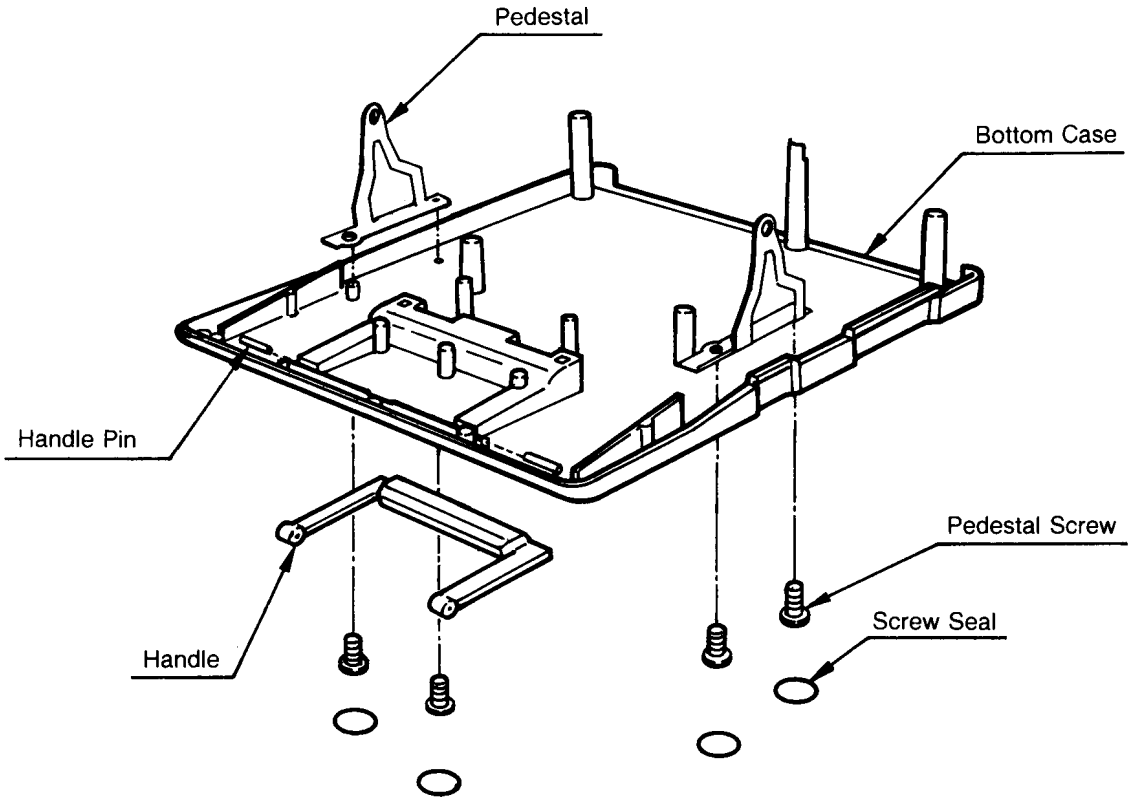


Figure 2-23. Bottom Case Dismantling

REMARK: Replacement of the Battery Pack

(1) Remove the Battery Cover by sliding it outward and take the Battery Pack out of the unit.
(2) Remove the connector and replace the Battery Pack. Stuff the cords between the Battery Pack and the Rear Panel so that they do not ride on the Battery Pack.

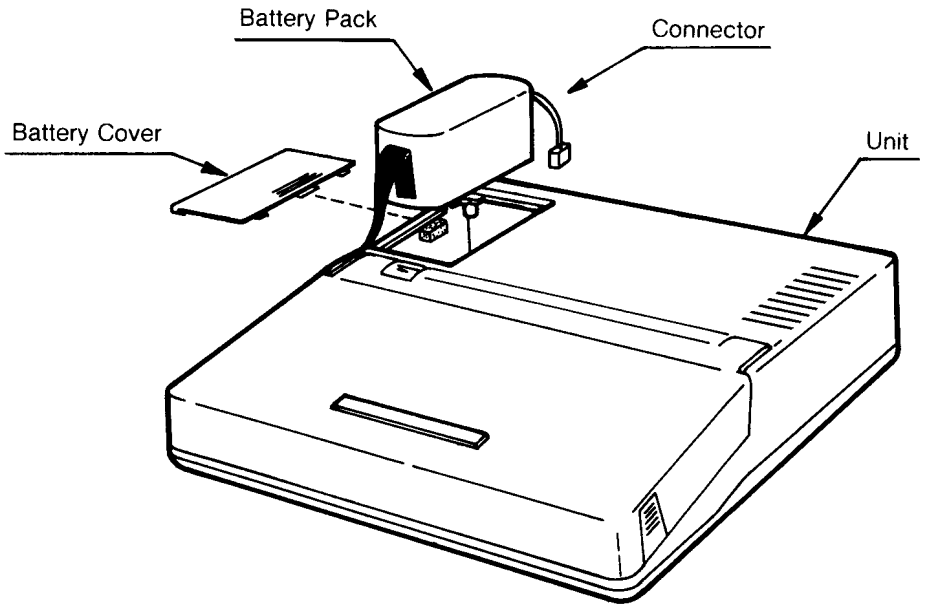


Figure 2-24. Battery Pack Replacement

The assembly procedure is the reverse of disassembly.

III. PREVENTIVE MAINTENANCE

III-1. To clean the body and LCD display

1. To avoid operational trouble, always keep the TANDY 1400LT clean.
2. Clean the body and the LCD screen using a soft, dry lint-free cloth.
3. For touch stains, clean the LCD screen with "Freon" 113
   Do not use any solvents other than "Freon"113.

III-2 RTC (Real Time Clock) Frequency Adjustment

1. Connect the measuring probes of a frequency counter to the Pin 3 (CKOUT) of IC36.
2. The oscillation frequency should be adjusted by altering the value of the trimmer capacitor (C51) using the standard 16.384 kHz clock signal output from the clock out (pin 3 of IC36) terminal.
3. Set up the TANDY 1400LT in MS-DOS: DEBUG MODE and enter the following command to generate the 16.384 kHz frequency.
   A>DEBUG
   - O 7D F9
   - O 70 01
4. Adjust C51 (trimmer capacitor) so as to read 16.384 kHz ±10 ppm on the frequency counter (If the frequency is not set to 16.384 kHz ±10 ppm level, the accuracy of the RTC can not be guaranteed ±5 minutes/month)

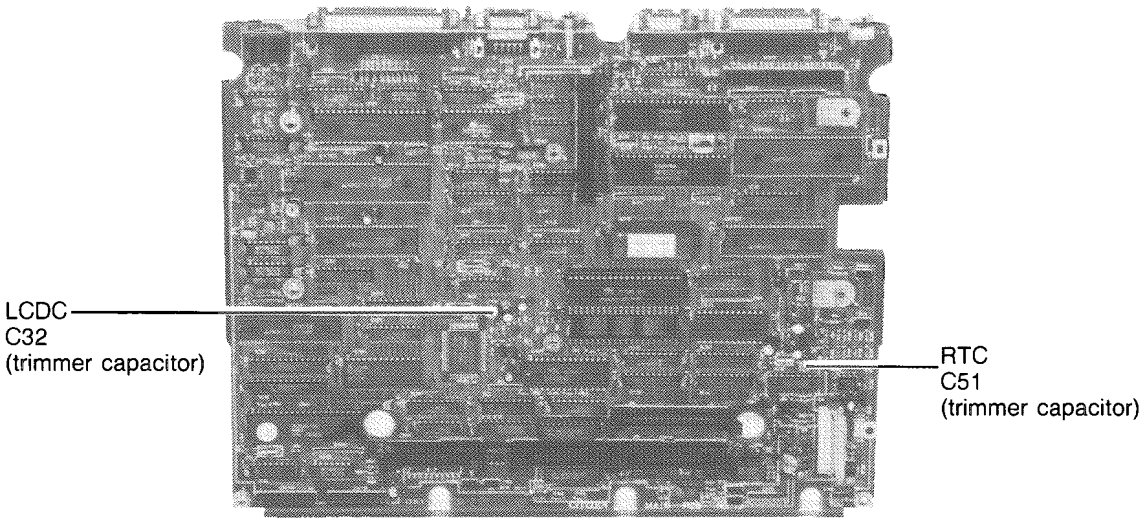


Figure 3-1. Frequency Adjustment

III-3. LCDC Frequency Adjustment

1. Connect the measuring probes of a frequency counter (high sensitivity and high input impedance) to the pin 65 of IC30.
2. Adjust C32 (trimmer capacitor) so as to read 21.47727 MHz on the frequency counter.

IV. THEORY OF OPERATION

IV-1 General

This section describes the theory of operation for the Tandy 1400LT. Figure 4-1 shows how this section is organized and highlights significant areas.

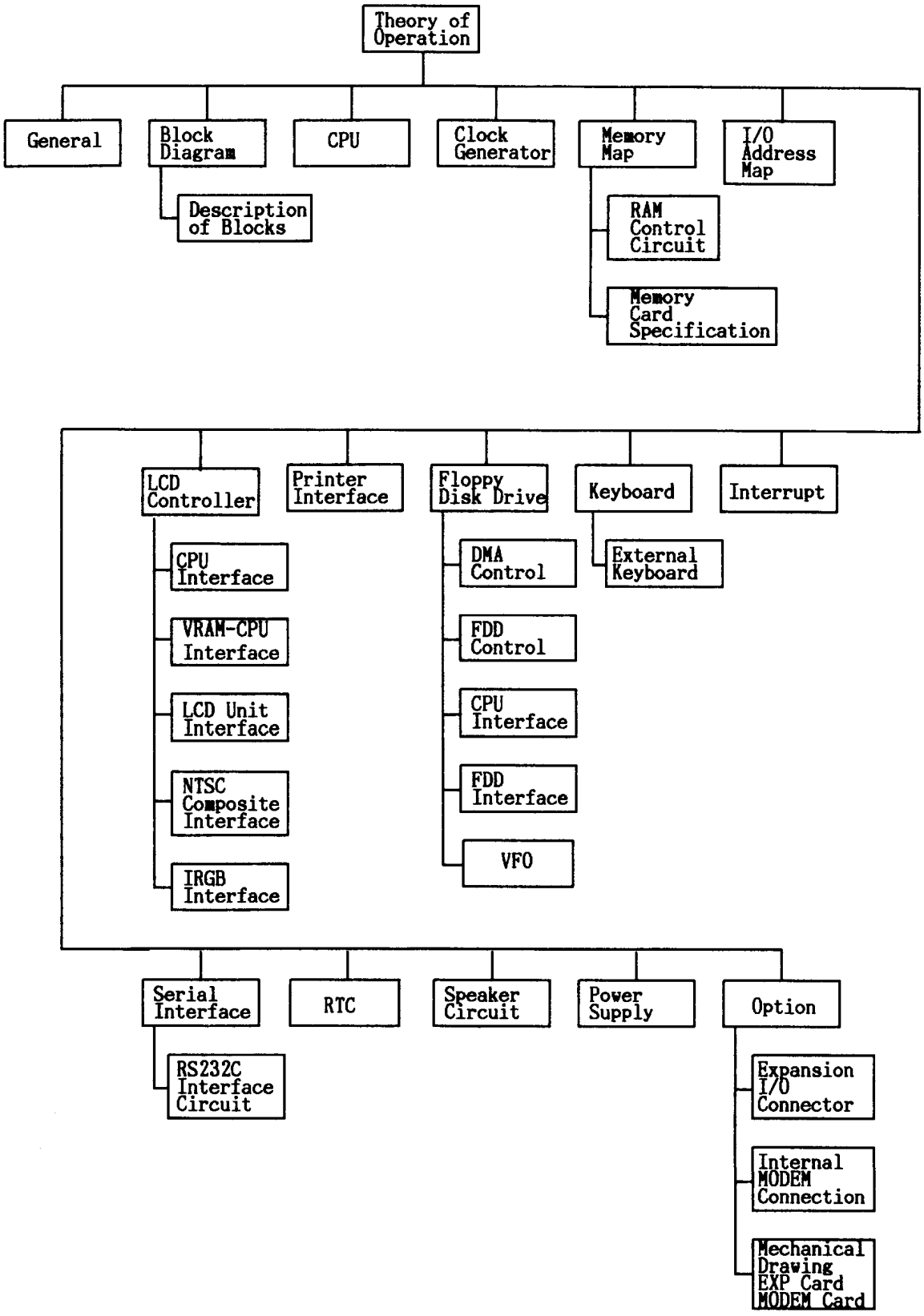


Figure 4-1. Organization of Section IV

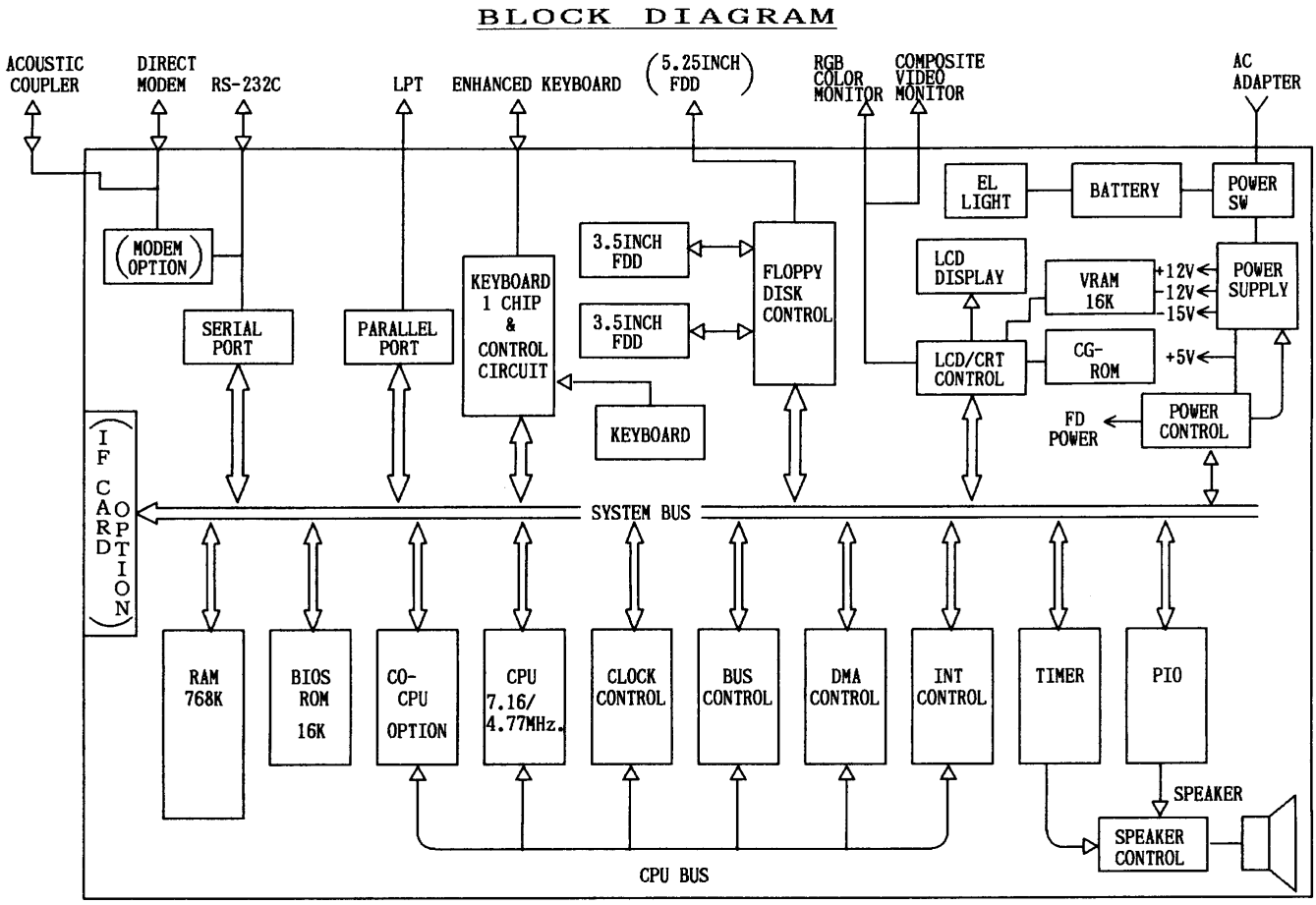


Figure 4-2. Block Diagram

IV-3. Description of Block Diagram

The Block Diagram of the TANDY 1400LT on the previous page shows the basic function divisions. The following are brief descriptions of the functions of each block.

CPU	NEC V20
CLOCK GENERATOR	Custom IC for dual clock speed
DMA CONTROL	82C37A-5 CMOS 4 Channel DMA controller (MAX DMA transmit speed 5MHz)
INTERRUPT CONTROLLER	71059C CMOS 8 channel interrupt controller.
BUS CONTROL	71088C CMOS bus controller. Manages bus arbitration.
TIMER/COUNTER	71054C CMOS 3 channel timer/counter
KEYBOARD/SENSE/CONTROL PORT	82C55 equivalent IC. Or use subset of 82C55.
INTERNAL KEYBOARD	76-Key full keyboard.
KEYBOARD CPU	80C49 Microprocesser to scan keys and transmit codes to system.
REAL TIME CLOCK	RICHO RP5C15
DISPLAY CONTROL	V6355
UART	TC8570P RS-232C interface
FDC	μPD72065C CMOS type of 765 floppy disk controller.
VFO	SED9420CAC
3.5 INCH FDD UNIT	3.5 inch double-sided,double-density front loading.

IV-4. CPU

The V20 is a CMOS 16-bit microprocessor provided with an 8/16 bit architecture and an 8 bit data bus. It has a powerful instruction set.

1. Packed BCD operation instruction.
2. High speed multiplication/division instruction.
3. Internal memory high speed block transfer.
4. Bit operation instruction.
5. High speed calculation of effective addresses.

The V20 is equipped with a 20-bit address bus that can access a 1M byte memory. In addition, the V20 has emulation functions of 8080 and comes with a standby mode that significantly reduces power consumption. The V20 can be used in two scale systems, the minimum mode, which is suitable for a small system, and the maximum mode, which is suitable for a large system. The microprocessor is configured in the TANDY 1400LT in the maximum mode.

IV-5. Clock Generator (Custom IC)

This custom-made IC (IC2) is a clock pulse generator/driver for microprocessors and their peripherals using high-speed CMOS technology. The custom-made IC has two speed MODE. The MODE is selectable by the level at pin 1 of IC2. The custom-made IC receives a 14.318MHz input clock and divides it by 2 to produce CPU "CLK" (7.16MHz : High speed MODE), and also divides it by 3 to produce CPU "CLK" (4.77MHz : Normal speed MODE). The custom-made IC also divides the same frequency by 6 and feeds the resulting 2.39MHz signal to the peripheral circuit to be used as the "PRCLK". In addition, to be used by the clock for DMA the custom-made IC produces 4.77MHz "DMACLK". The "OSC" (pin 12 of IC2) outputs a signal at the same frequency as the crystal input. (All clocks are 50% duty cycle)

MODE	NORMAL SPEED	HIGH SPEED
OSC	14.318 MHz	14.318 MHz
CLK	4.77 MHz	7.16 MHz
PRCLK	2.39 MHz	2.39 MHz
DMACLK	4.77 MHz	4.77 MHz
LEVEL at Pin 1 of IC2	High	LOW

Table 4-1. Clock Speed

When the power is turned on, the CPU and the peripheral circuits are reset by IC2 using " $\overline{\text{RESIN}}$" signal (this Schmitt-trigger input generates the "RESET" output). Reset timing is provided by " $\overline{\text{RESIN}}$" input to Schmitt-trigger input gate and flip-flop which will synchronize the reset timing to the falling edge of "CLK".
Figure 4-3 Clock-Gen.1 Shows the IC 2 Pin-out.

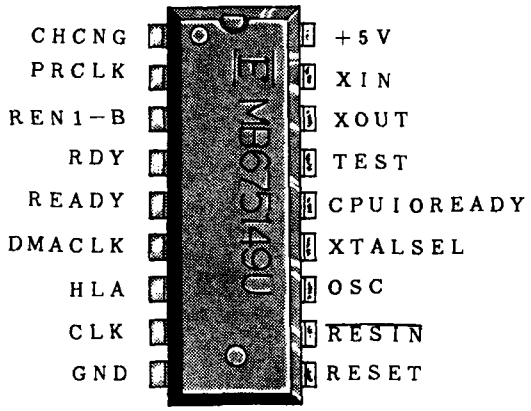


Figure 4-3. Clock-Gen.1

Figure 4-4 Clock-Gen.2 shows IC2 and peripheral circuitry.
Figure 4-5 Clock-Gen.3 shows internal logic block diagram of IC2.

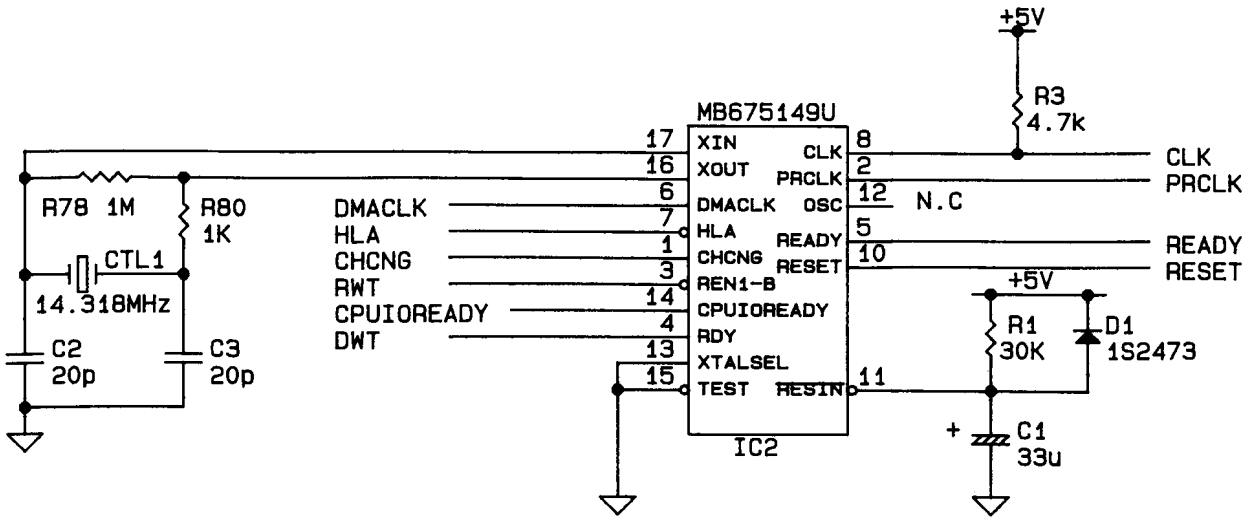


Figure 4-4. Clock-Gen.2

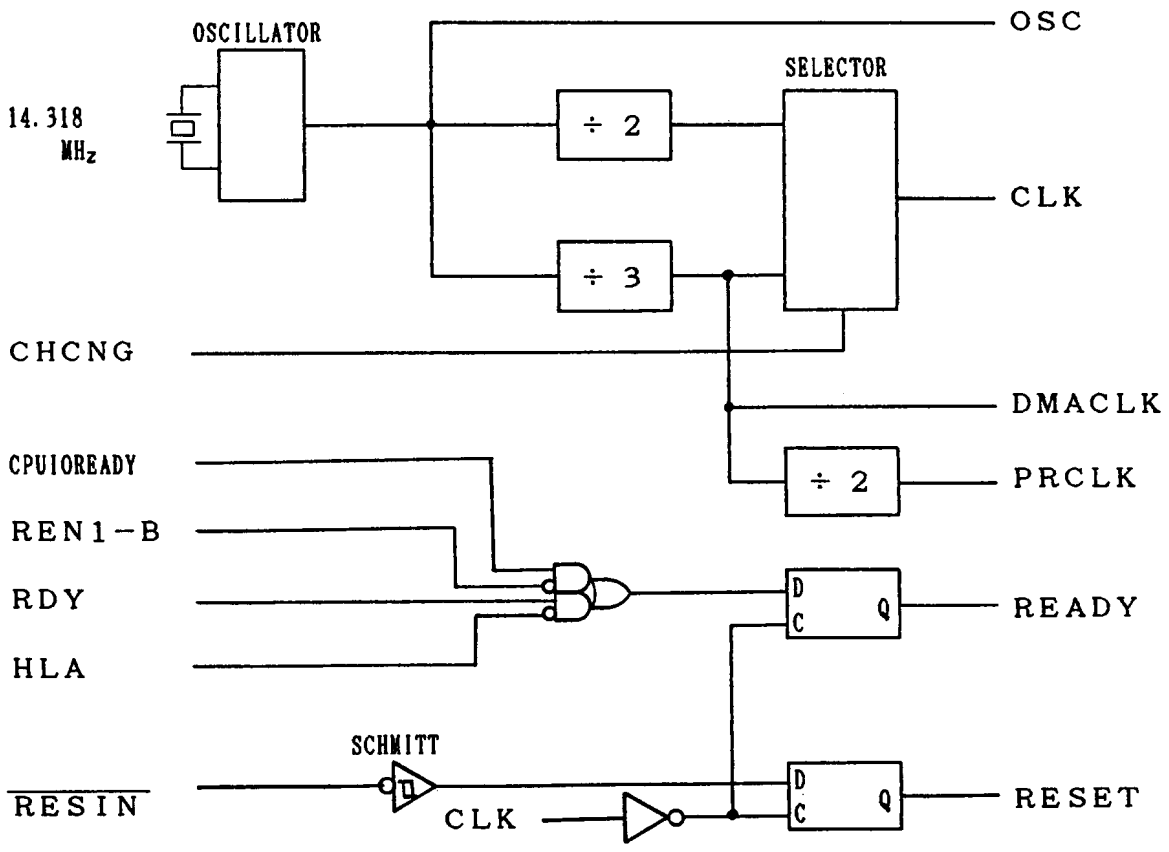


Figure 4-5. Clock-Gen.3

Figure 4-6 Clock-Gen.4 shows 1. Clock mode change timing operation. 2. RESET timing operation. and 3. READY timing operation.

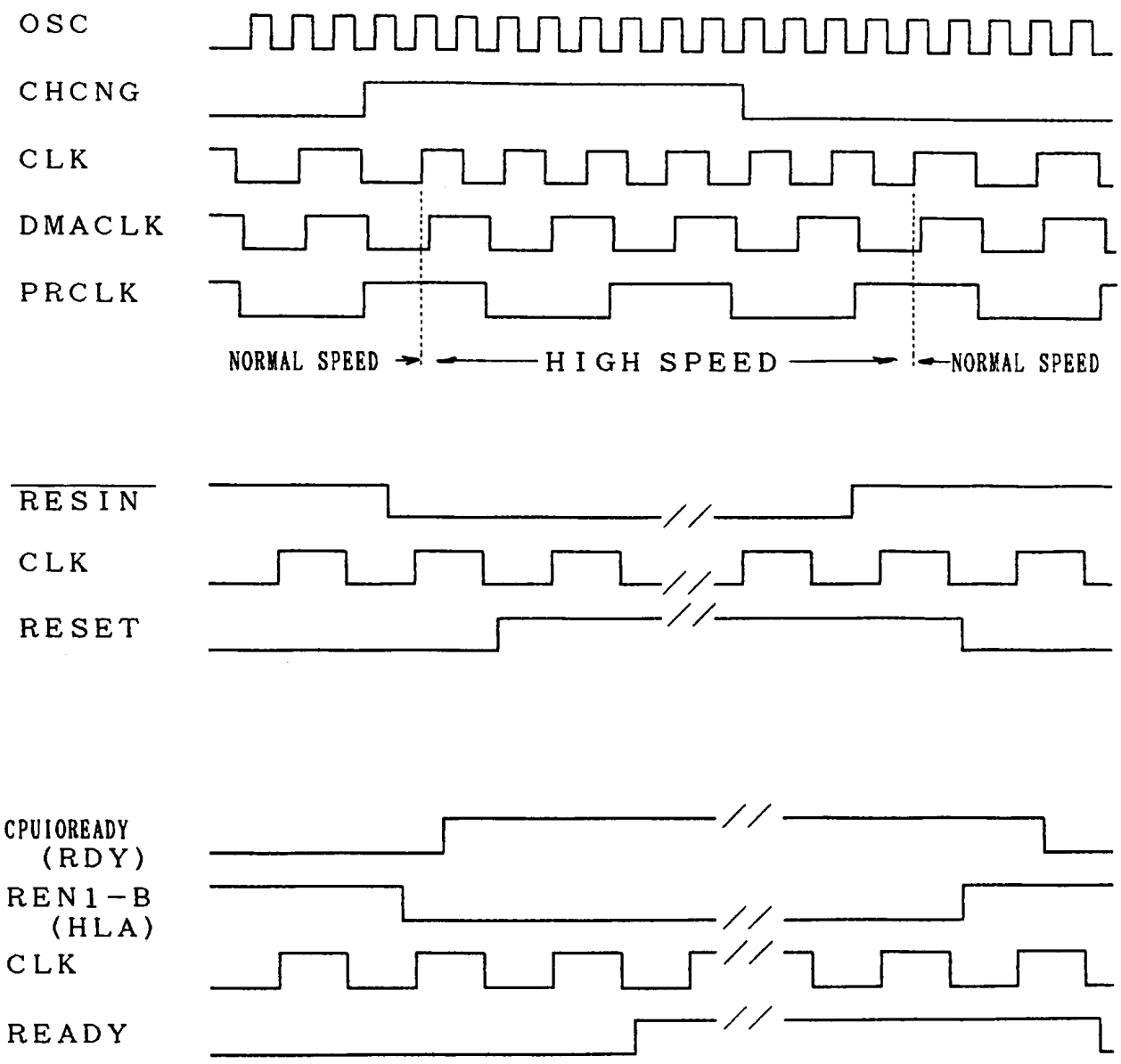


Figure 4-6. Clock-Gen.4

IV-6. MEMORY MAP

Figure 4-7 Memory-Map shows the location on the board of the IC and the corresponding memory Column-Address Strobe ($\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$)
(40000H -9FFFFH and DC000H -FBFFFH addresses are enabled or disabled by DIP switch (DS1)).

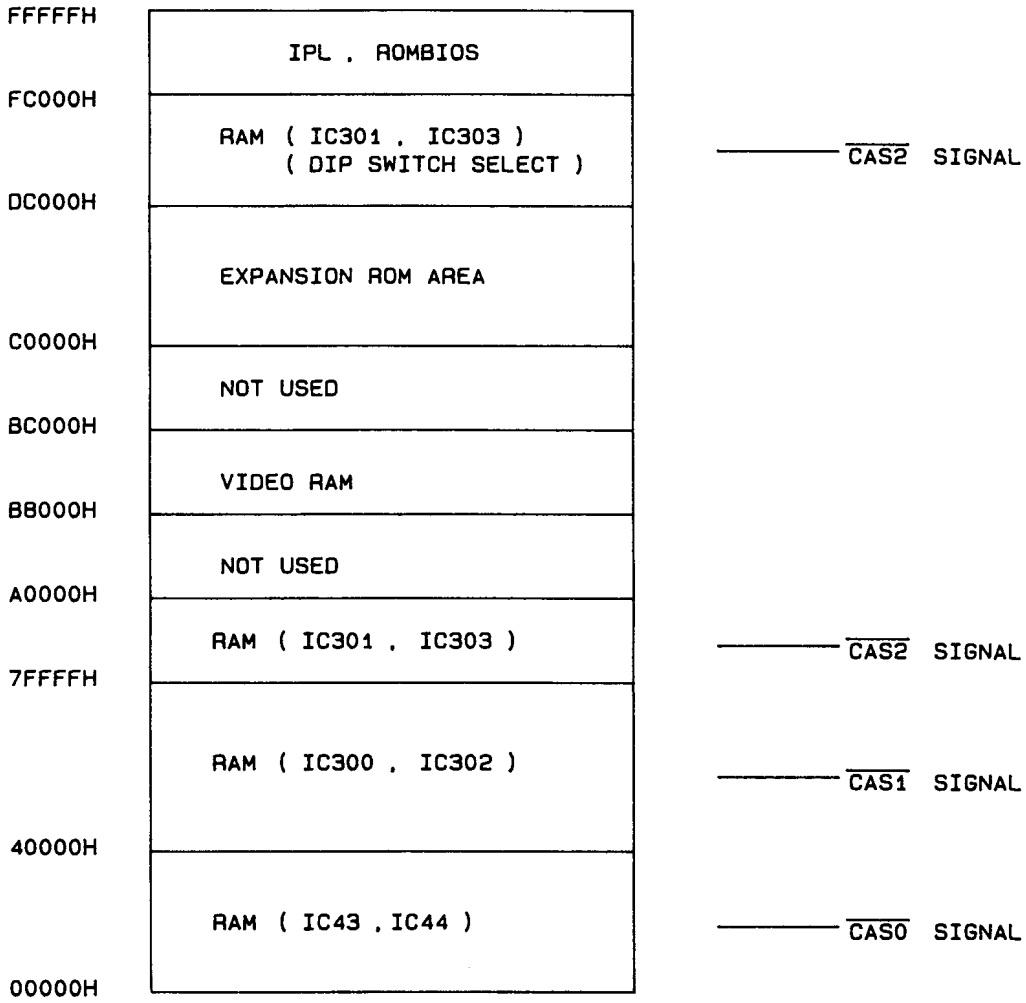


Figure 4-7. Memory-Map

Figure 4-9 shows the switch settings and description.

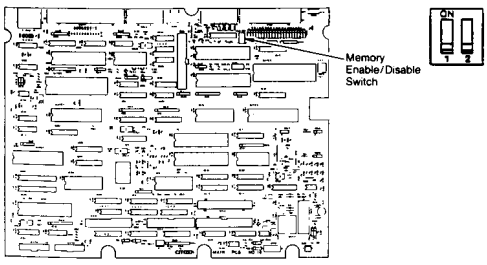


Figure 4-8. DIP-SW Location

DIP SWITCH		Function	Description
DIP SW	Setting		
SW 1	OFF ON	Internal/External use address 4000:0-9000:FFFF	Internal use External use
SW 2	OFF ON	Internal/External use address DC00:0-EC00:FFFF	Internal use External use

Figure 4-9. DIP-SW

IV-7. RAM Control Circuit

Figure 4-10 shows the DRAM refresh control block diagram. The TANDY 1400LT uses the Timer/Counter (IC21) and DMAC (IC18) for DRAM refresh. About every 15usec, a pulse is generated by the Timer/Counter (IC21) and it raises up DR0 (DMA Request channel 0) signal. And then DMAC (IC18) counts up the address for DRAM refresh. Column-address strobe is generated in GATE2. Figure 4-11 shows the circuit of "0" active $\overline{CAS0}$, $\overline{CAS1}$ and $\overline{CAS2}$ signal generators.

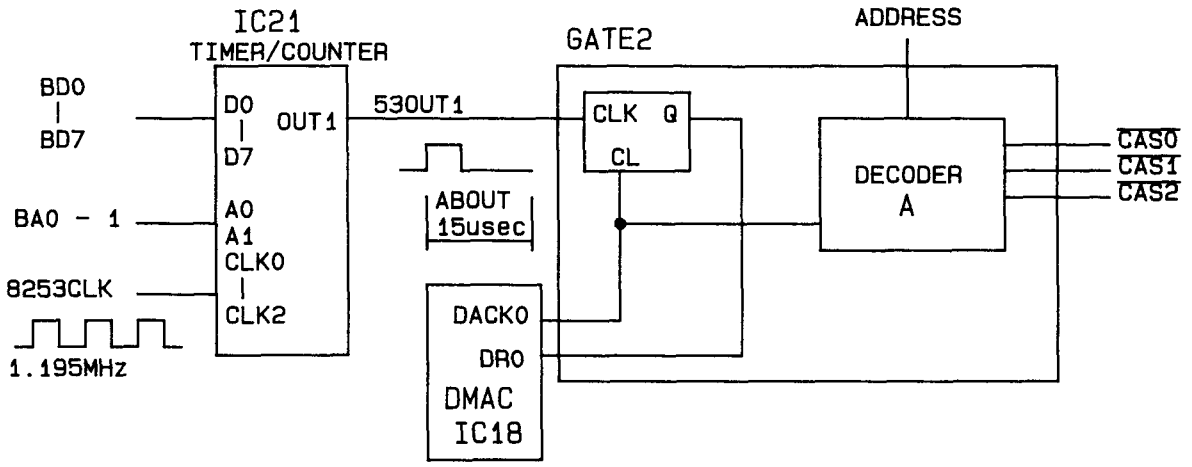


Figure 4-10. RAM-1

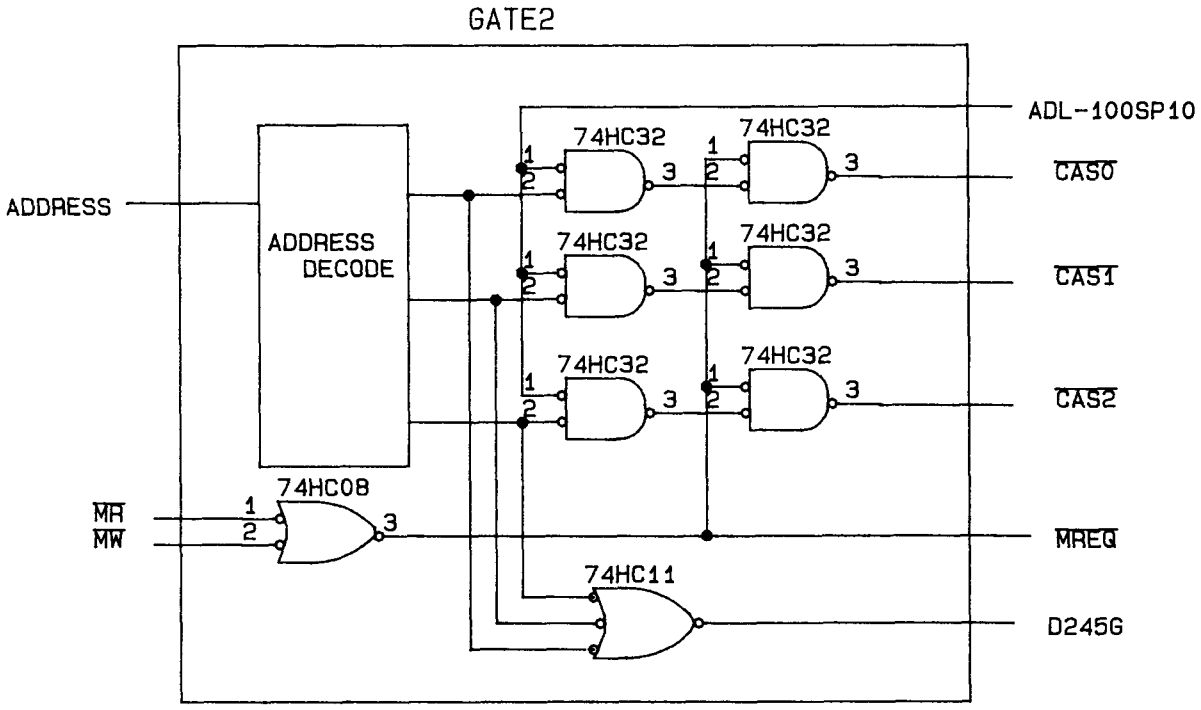


Figure 4-11. RAM-2

Figure 4-12 RAM-3 shows the DRAM and peripheral circuitry.
ADL-100SP10 signal is generated by the IC45 (Active time delay line) and it affects Column-address-strobe timing. ($\overline{CAS0}$, $\overline{CAS1}$, and $\overline{CAS2}$)

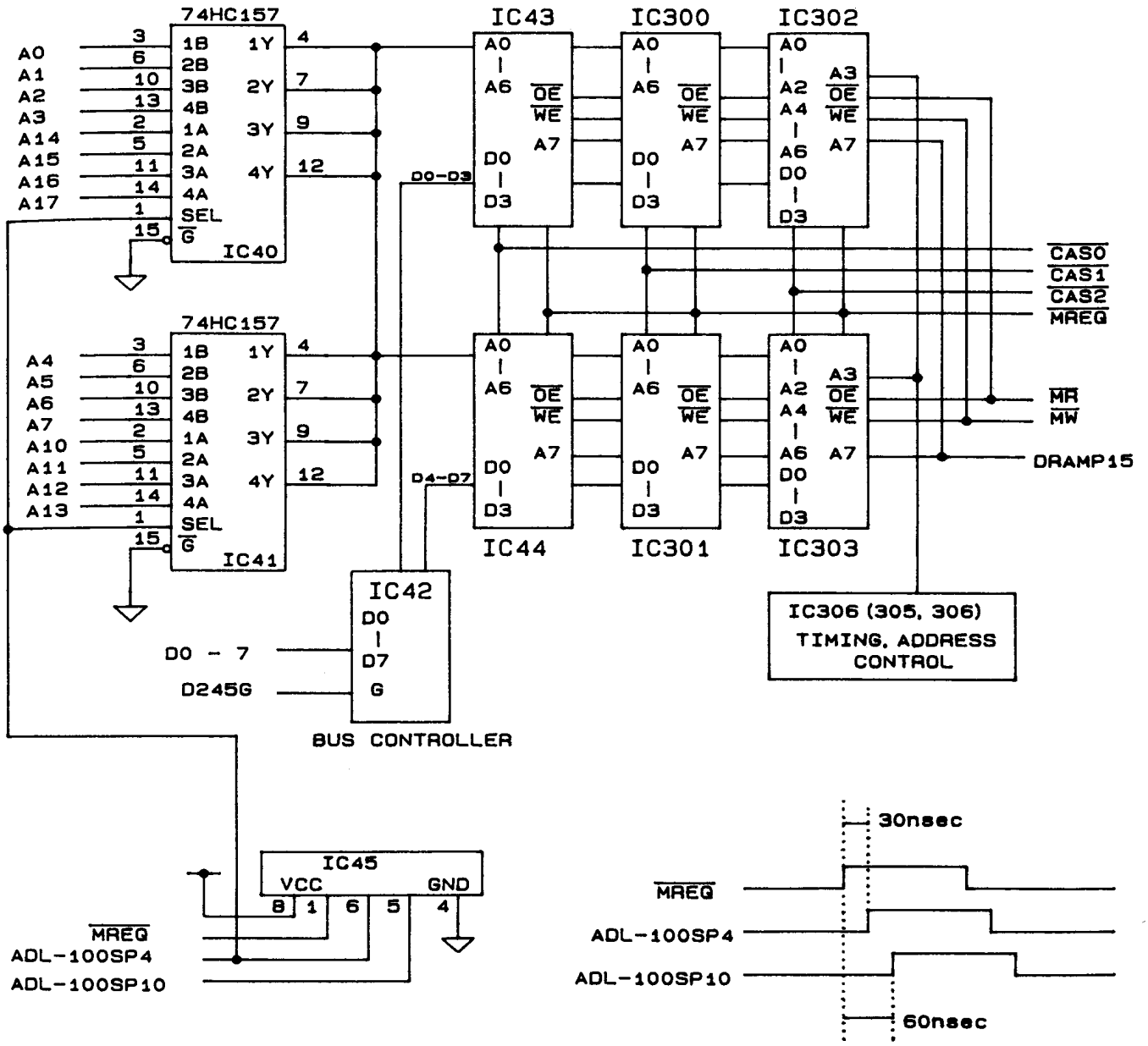


Figure 4-12. RAM-3

Memory device location.
IC43 , IC44 –On the Main PCB
IC300 - 303 –On the RAM PCB →

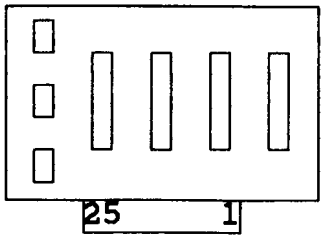


Figure 4-13. Memory-Card

IV-8. Memory Card Specification

1. Maximum RAM configuration becomes 512K bytes (IC300,301,302,303)
2. Device
   Memory –1Mbit DRAM (256Kbit by 4 type)
   High speed CMOS –74HC04, 74HC08
   Active delay line
3. Pin assignment
   Right side of PCB parts-side is pin No. 1.

Table 4-2 Memory-Card shows the Memory Card pin assignments.

Pin Number	Signal Name	Contents
1	EMA0	Actual address A0 & A14
2	EMA1	Actual address A1 & A15
3	EMA2	Actual address A2 & A16
4	EMA3	Actual address A3 & A17
5	EMA4	Actual address A4 & A10
6	EMA5	Actual address A5 & A11
7	EMA6	Actual address A6 & A12
8	EMA7	Actual address A7 & A13
9	DRMAP15	Actual address A8 & A9
10	EMD0	Data I/O -D0
11	EMD1	Data I/O -D1
12	EMD2	Data I/O -D2
13	EMD3	Data I/O -D3
14	EMD4	Data I/O -D4
15	EMD5	Data I/O -D5
16	EMD6	Data I/O -D6
17	EMD7	Data I/O -D7
18	*EMR	Memory read signal
19	*EMW	Memory write signal
20	*CAS1	Column address strobe (4000:0-7000:FFFF)
21	*CAS2	Column address strobe (8000:0-9000:FFFF) (DC00:0-EC00:FFFF)
22	A18	Address 18
23	GND	
24	+5V	
25	GND	
26	+5V	

Table 4-2. Memory-Card

IV-9. ROM Control Circuit

"0" active $\overline{\text{CSRO}}$ signal is chip enable signal for ROM ($\overline{\text{CE}}$). It is decoded in the GATE2. Figure 4-14 shows the address decoder circuit. Figure 4-15 shows the ROM and peripheral circuitry.

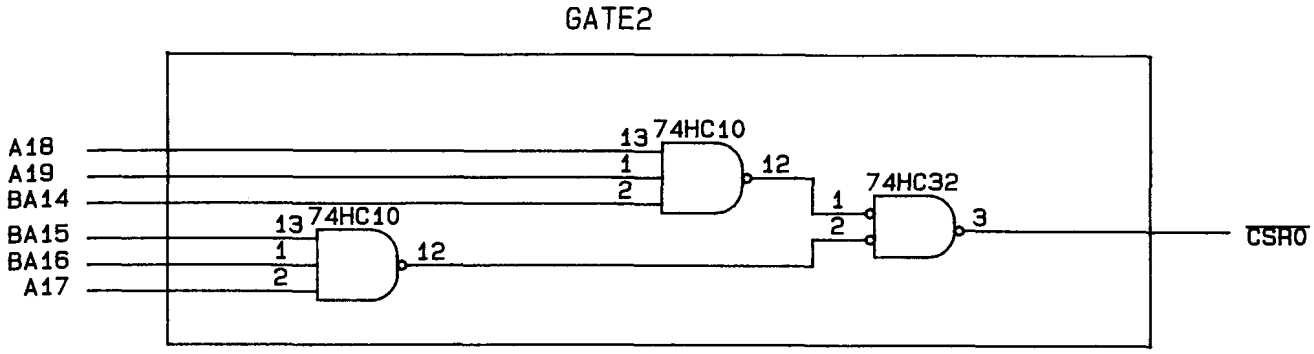


Figure 4-14. ROM Address Decoder Circuit

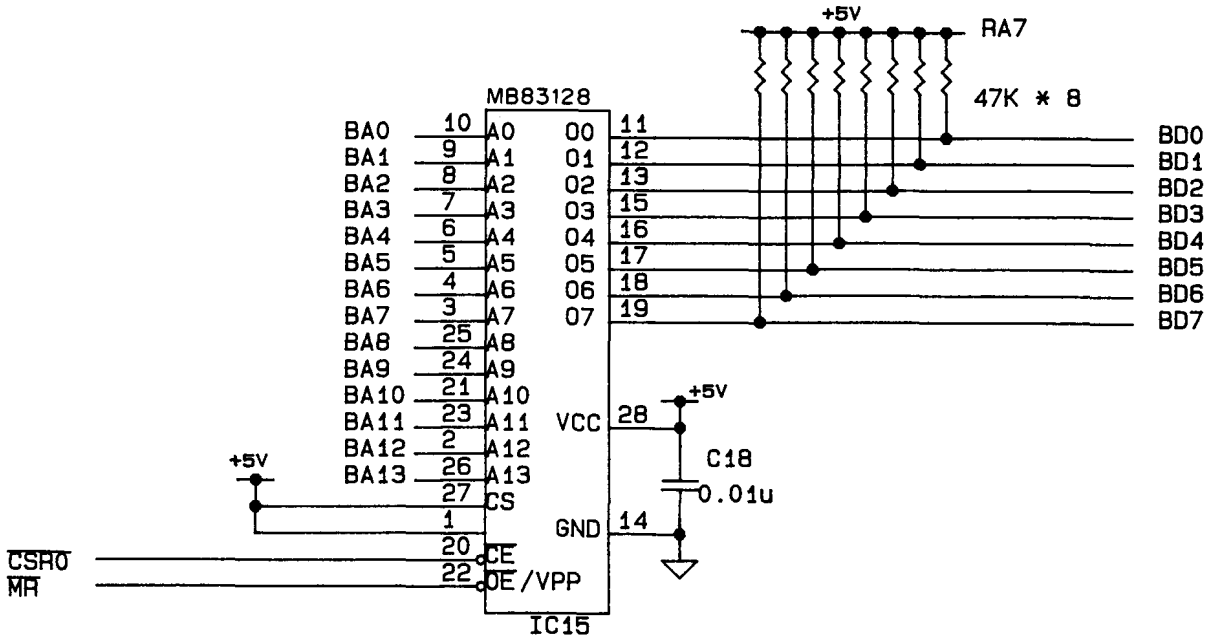


Figure 4-15. ROM and Peripheral Circuitry

IV-10. I/O Address Map

ADDRESS	BIT	CONTENTS	CONTROL
DMA CONTROLLER			
08H		37 Command Register	Command & Status
09H		37 Request Register	Write only
0AH		37 Mask Register	Write only
0BH		37 Mode Register	Write only
0CH		37 Clear First/Last FF	Write only
0DH		37 Temp Reg/Master clear	R=Temp Register
0EH		37 Clear Mask Register	Write only
0FH		37 All Mask Register	Write only
INTERRUPT CONTROLLER			
020H		59 Register	IRR & ISR
021H		59 Register	IMR
TIMER/COUNTER			
040H		53 Counter 0	Interrupt Request 0
041H		53 Counter 1	For DRAM Refresh
042H		53 Counter 2	Beep
KEYBOARD/SENSE/CONTROL		PORT	
060H	0	Keyboard Bit 0	Port A
	1	Keyboard Bit 1	
	2	Keyboard Bit 2	
	3	Keyboard Bit 3	
	4	Keyboard Bit 4	
	5	Keyboard Bit 5	
	6	Keyboard Bit 6	
	7	Keyboard Bit 7	
061H	0	Gate A Timer Chip for Speaker Tone Output	Port B
	1	Enable Speaker	
	2	Open for other uses	
	3	Read High switches or Read Low switches.	
	4	Open for other uses	
	5	Open for other uses	
	6	Keyboard buffering SW.	
	7	Keyboard interrupt reset	
062H	0	System status of hardware	Port C
	1	System status of hardware	
	2	System status of hardware	
	3	System status of hardware	
	4	Open for other uses	
	5	To test Timer output	
	6	I/O channel check (always low level)	
	7	RAM parity check (always low level)	
REAL TIME CLOCK			
070H ∫ 07FH		Real Time Clock Register	

Table 4-3. I/O Address Map

ADDRESS	BIT	CONTENTS	CONTROL
DMA PAGE REGISTER			
080H		Not used	
081H		DMA Page Register for DMA Channel 2	
082H		DMA Page Register for DMA Channel 3	
083H		DMA Page Register for DMA Channel 1	
NMI MASK REGISTER			
0A0H	7	NMI Mask Register	
SYSTEM STATUS REGISTER			
0F8H	0	Loop on post	
	1	Co-processor installed	1/active , 0/not
	2	RAM Size	00/Not means,01/640K
	3	RAM Size	10/512K, 11/256K
	4	Display 0	00/reserved
	5	Display 1	01/Color 40*25 10/Color 80*25 11/Monochrome
	6	Number of FDD	00/1 , 01/2
	7	Number of FDD	10/3 , 11/4
(Write Register)			
0FAH	0	LCD/CRT Exchange	1/CRT , 0/LCD
	1	FD Power Control	1/ON , 0/OFF
	2	LCD Power Control	1/ON , 0/OFF
	3	EL Back Light Control	1/ON , 0/OFF
	4	Keyboard Select Switch	1/EXT , 0/INTERNAL
	5	CRT Controller Disable	1/DIS , 0/ENABLE
	6	Not used	
	7	Low Battery 1 NMI MASK	0/MASK
(Read Register)			
0FAH	0	LCD/CRT Switch Status	1/CRT , 0/LCD
	1	FD Power Status	1/ON , 0/OFF
	2	LCD Power Status	1/ON , 0/OFF
	3	EL Back Light Status	1/ON , 0/OFF
	4-7	Not used	
(Write Register)			
0FCH	0	Power Save Control	1/ON , 0/OFF
	1	Modem Power Control	1/ON , 0/OFF
	2	Modem/RS-232C Switch	1/MODEM,0/RS-232C
	3	Speaker Power Control	1/ON , 0/OFF
	4	Direct/Acoustic Switch	1/Direct,0/Acoustic
	5	Clock Speed Exchange	1/7.16 , 0/4.77MHz
	6	Not used	
	7	Low Battery 2 NMI MASK	0/MASK

Table 4-3. I/O Address Map (Cont.)

ADDRESS	BIT	CONTENTS		CONTROL
PRINTER CONTROL				
378H		Printer Data Output Port		
379H		Printer Status Port		
37AH		Printer Control Port		
VIDEO CONTROLLER				
3D0H				
∫		V6355 Control Registers		
3DFH				
FLOPPY DISK CONTROLLER				
3F2H	0	Drive Select		00/DRIVE A
	1	Drive Select		01/DRIVE B
				10/DRIVE C
				11/DRIVE D
	2	Not FDC Reset		
	3	Enable INT & DMA Request		
	4	Drive A Motor ON & In-use		1/ON , 0/OFF
	5	Drive B Motor ON & In-use		1/ON , 0/OFF
	6	Drive C Motor ON & In-use		1/ON , 0/OFF
	7	Drive D Motor ON & In-use		1/ON , 0/OFF
3F4H		FDC Main Status Register		
3F5H		FDC Data Register		
COM1 CONTROL				
3F8H(Write)		Tx Buffer	(DLAB=0)	
3F8H(Read)		Rx Buffer	(DLAB=0)	
3F8H		Divisor Latch LSB	(DLAB=1)	
3F9H		Divisor Latch MSB	(DLAB=1)	
3F9H		Interrupt Enable Register	(DLAB=0)	
3FAH		Interrupt Identification Registers		
3FBH		Line Control Register		
3FCH		Modem Control Register		
3FDH		Line Status Register		
3FEH		Modem Status Register		

Table 4-3. I/O Address Map (Cont.)

IV-11. Interrupt

The V20 has abundant interrupt processing functions:
External interrupt : NMI (Non-maskable interrupt)
INT (Maskable interrupt)
Interrupt by software

The 71059C Interrupt Controller is the source of the INT for the CPU. It is a low-power CMOS programmable interrupt control unit. It can process eight interrupt request inputs, allocating a priority level to each one.

Interrupt controller Channel Assignment

IRQ 0 - Timer interrupt for relative timer.
IRQ 1 - Keyboard interrupt.
IRQ 2 - Open for other uses.
IRQ 3 - Open for other uses.
IRQ 4 - COM 1 interrupt.
IRQ 5 - Open for other uses.
IRQ 6 - Floppy Disk Controller interrupt.
IRQ 7 - Printer interface interrupt.

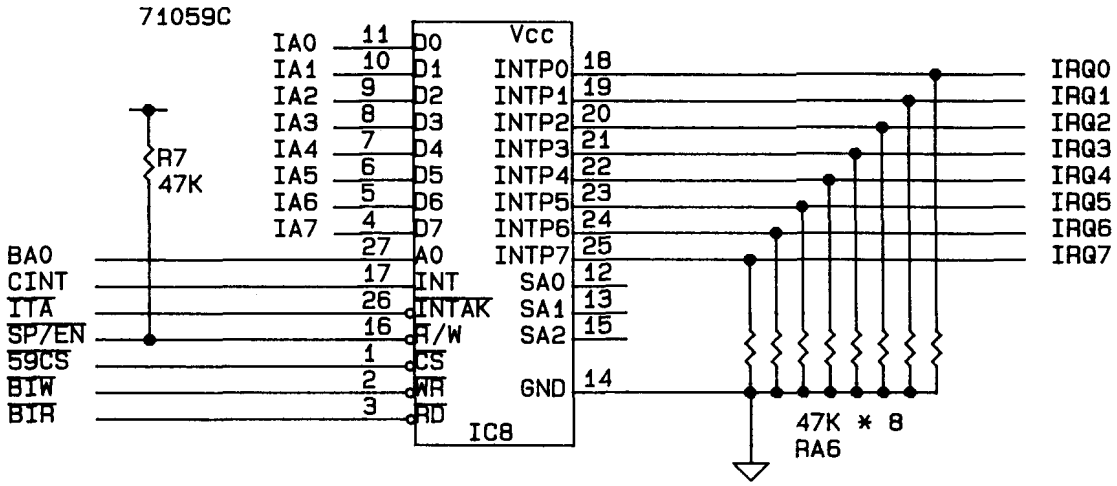


Figure 4-16. 71059C and Peripheral Circuitry

There are three NMI-interrupt sources in the TANDY 1400LT

1. NMI from Co-processor
2. Low battery1
3. Low battery2

The Low battery1 and Low battery2 are signals for battery voltage warning. The Low battery1 signal become active at a battery voltage 11.7V - 11.9 V. After Low battery1 signal become active, the system can be used for about 30 minutes with the FDD 10% duty. Then Low battery2 signal will become active. (The Low battery1 and Low battery2 signals are maskable by the I/O ports 0FAH and 0FCH. Refer to I/O address map.)
The NMI interrupt is not maskable by the CPU, but it can be enabled or disabled by the hardware. The enable-state is activated by port 0A0H bit 7. The enable-state is cleared by RESET.

IV-12. Keyboard

The TANDY 1400LT can use an Internal keyboard and an External keyboard.
Figure 4-17 shows the block diagram in GATE4. The data from Internal keyboard is a parallel 8-bit data, and from External keyboard is a serial 10 bit data. The data is selected in GATE4 (selector A) and goes to the data bus through I/O port 060H (subset of 82C55). Internal keyboard is controlled by IC50. IC50 is a single chip, 8-bit microprocesser containing an 8-bit CPU, ROM, RAM, I/O ports and control circuitry. IC50 generates strobe signal at every key-stroke.(KP21)
Figure 4-18 shows IC50 and peripheral circuitry.

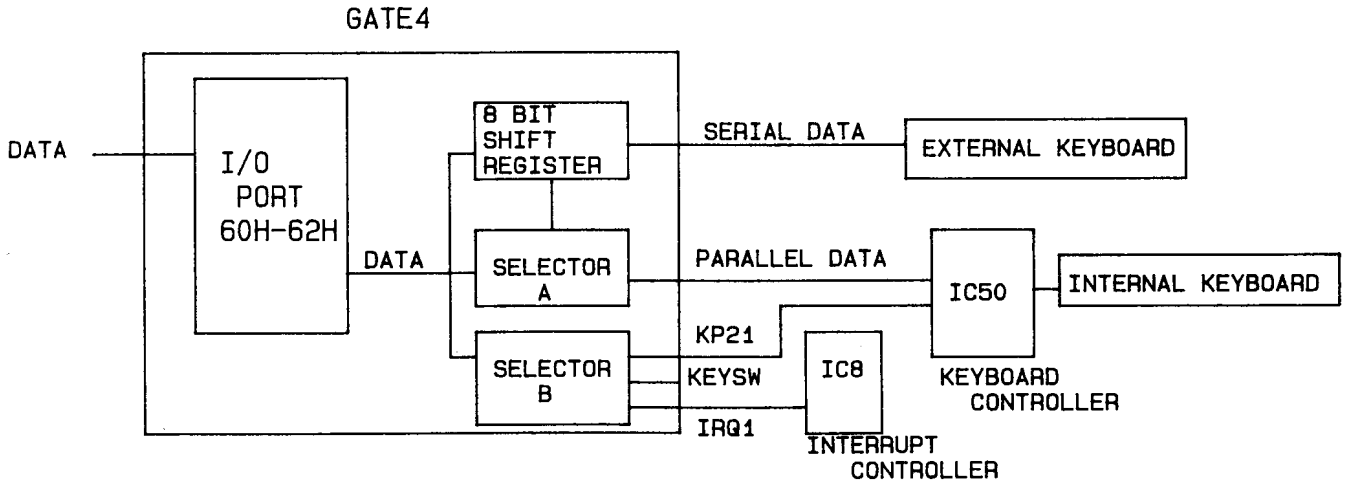


Figure 4-17. Keyboard-1 (The Block Diagram in the GATE4)

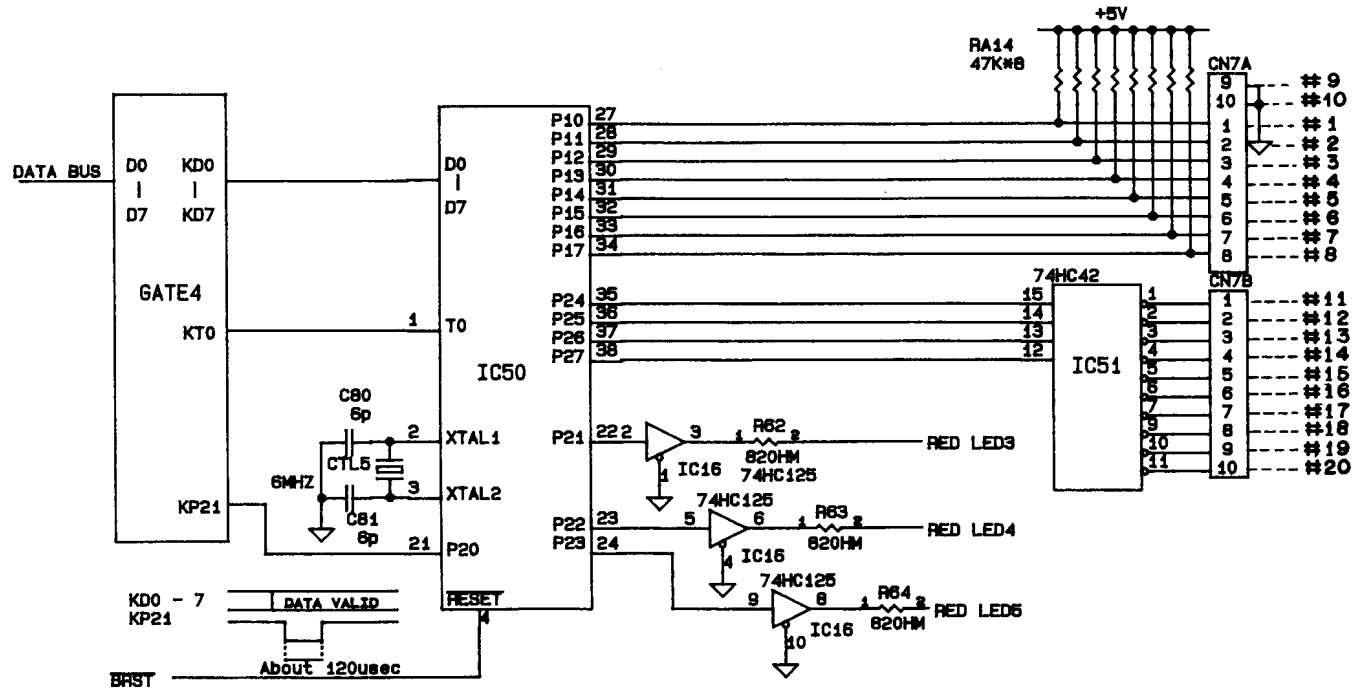


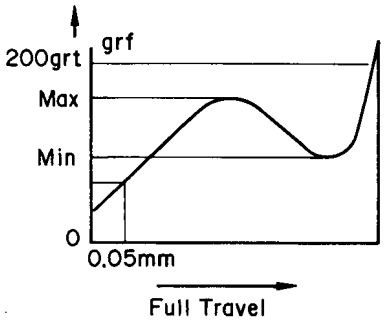
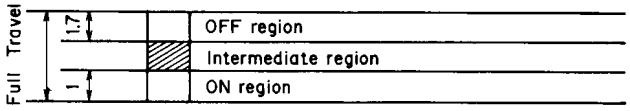
Figure 4-18. Keyboard-2 (IC50 and Peripheral Circuitry)

Figure 4-19, 4-20 KEYBOARD-3, -4 show internal keyboard specification

Electrical Specifications

1	Maximum Rating	12 V DC, 5 mA
2	Contact Bounce	5 m sec. Max (at normal pushing)
3	Contact Resistance	300 m Ohm Max. (at 10 million times operation, -5 Ohm Max.)
4	Insulation Resistance	50 m Ohm Min. (at 250 V DC)
5	Withstand Voltage	250 V AC, 1 minute
6	Circuit	Make contact, 1 circuit

Mechanical Specifications

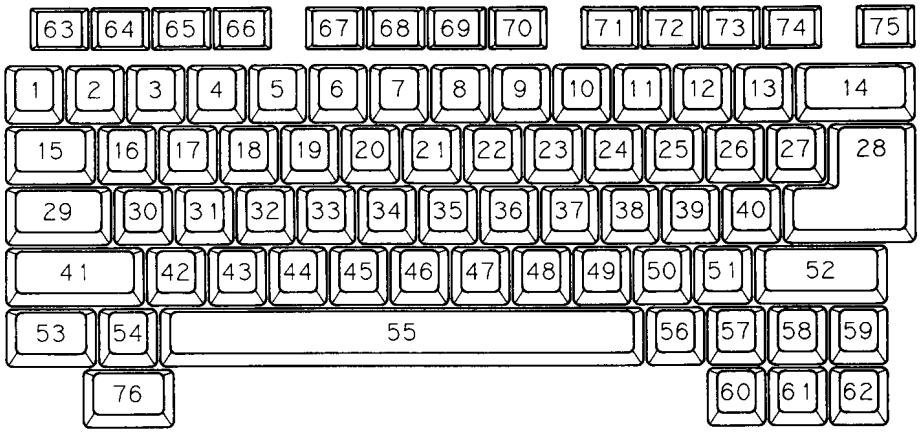
1	Operation Force (MAX: first stage life stage (MIN:	35 grf 50 ± 150 grf 40 ± 15 grf) 26 ± 19 grf)	
2	Full Travel	4.0 ± 0.5 mm	
3	Operating Point		

Endurance Specifications

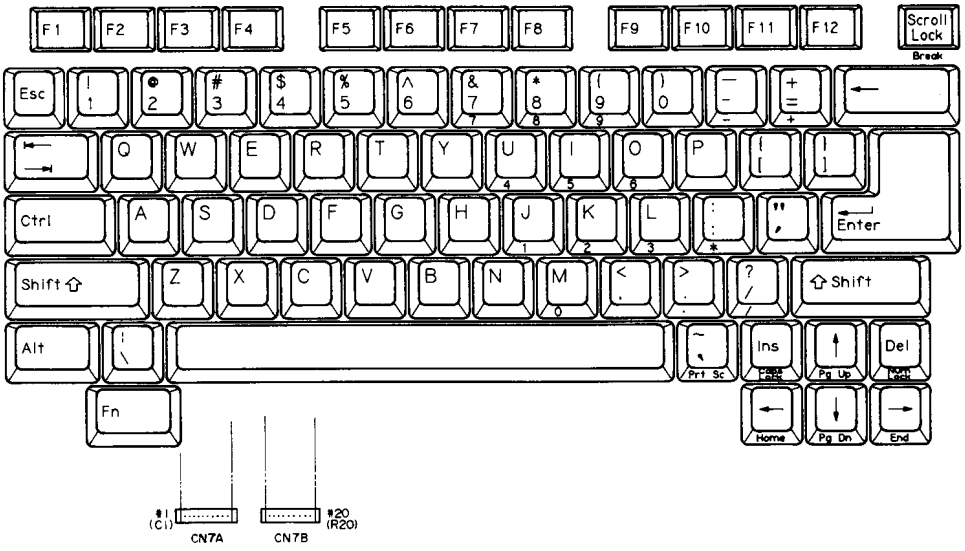
1	Operation Life	12V DC 5mA	10,000,000 times
		24V DC 10 mA	5,000,000 times
2	Operation Temperature Range		−5°C ~ +5°C
3	Storage Temperature Range		−20°C ~ +65°C

Figure 4-19. KEYBOARD-3 (Internal Keyboard Specification)

Key-position No.

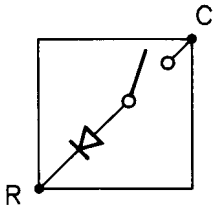


Keyboard Layout (for U.S.A.)



Key Matrix (for U.S.A.)

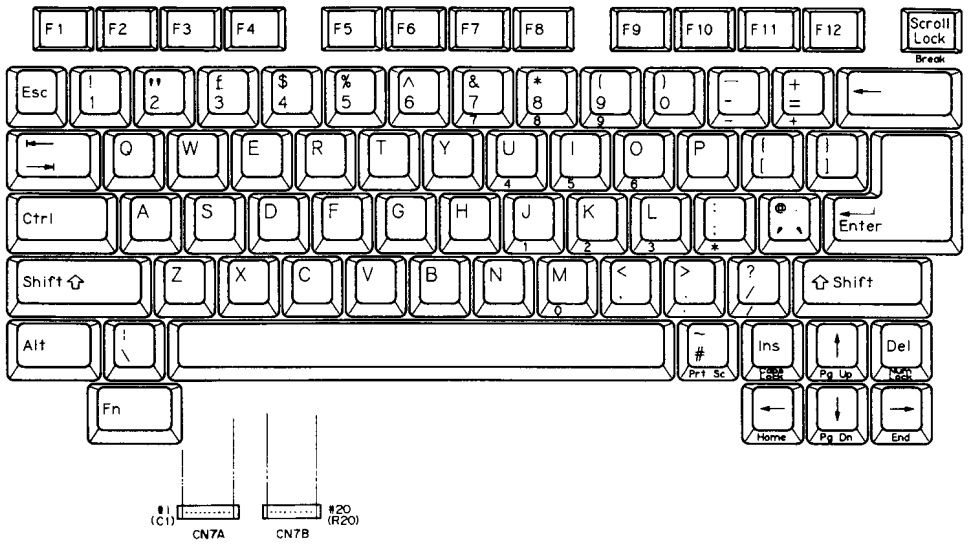
	C1	C2	C3	C4	C5	C6	C7	C8	C9	C10
R11	) 0	! 1	@ 2	# 3	$ 4	% 5	^ 6	& 7	NC	
R12	* 8	(9	— -	+ =	: \	{ [	}]	: ;		
R13	" '	~ `	< ,	> .	? /		A	B		
R14	C	D	E	F	G	H	I	J		
R15	K	L	M	N	O	P	Q	R		
R16	S	T	U	V	W	X	Y	Z		
R17	SP				Home ←	Pg Up ↑	Pg Dn ↓	End →		
R18	Esc	⇤ ⇥	BS	Enter	F9	F10	F11	F12		
R19	F1	F2	F3	F4	F5	F6	F7	F8		
R20	Alt	Ctrl	Shift⇧	⇧Shift Prt Sc	Fn	Ins	Del	Scroll Lock		



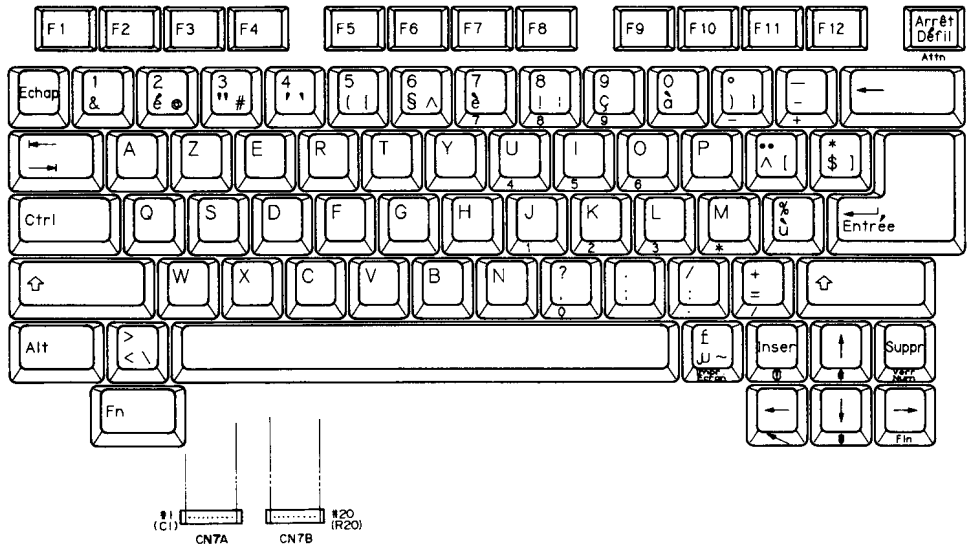
Switch Detail

Figure 4-20. Keyboard-4 (Position, Layout and Matrix)

Keyboard Layout (for U.K.)



Keyboard Layout (for France)



Keyboard Layout (for Italy)

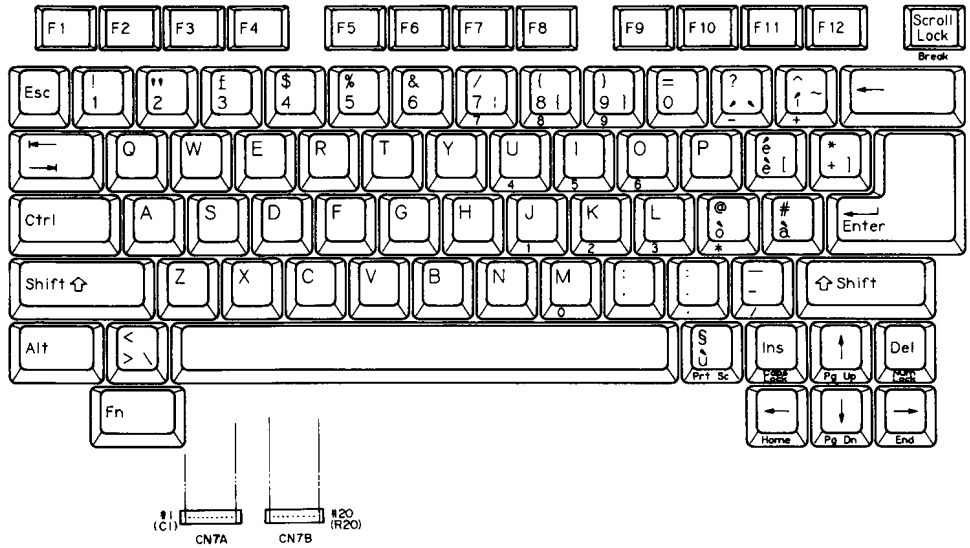
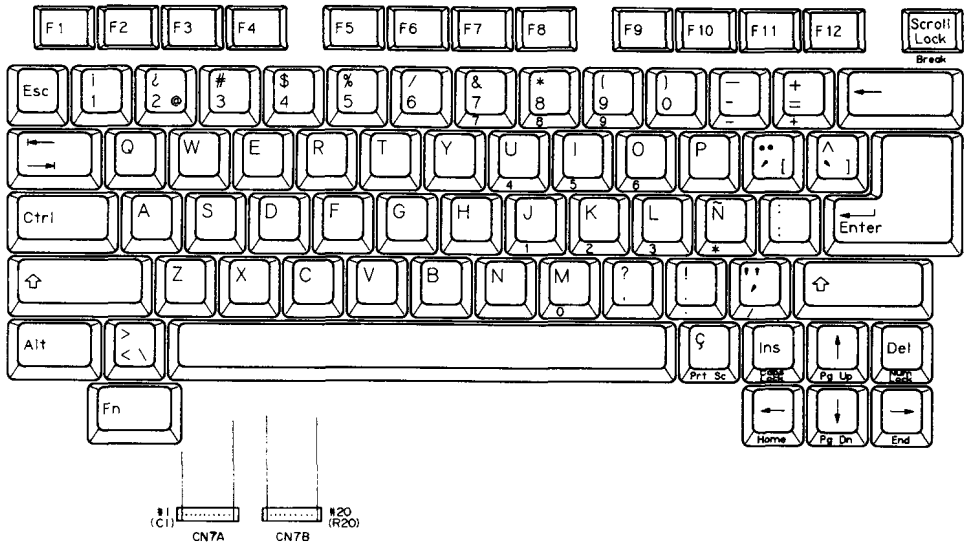
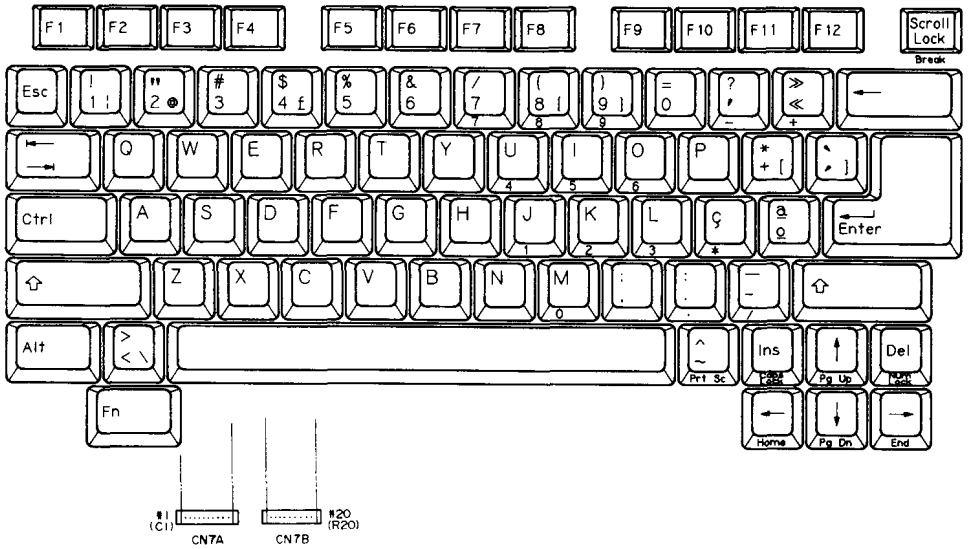


Figure 4-20. Keyboard-4 (Cont.)

Keyboard Layout (for Spain)



Keyboard Layout (for Portugal)



Keyboard Layout (for Belgium)

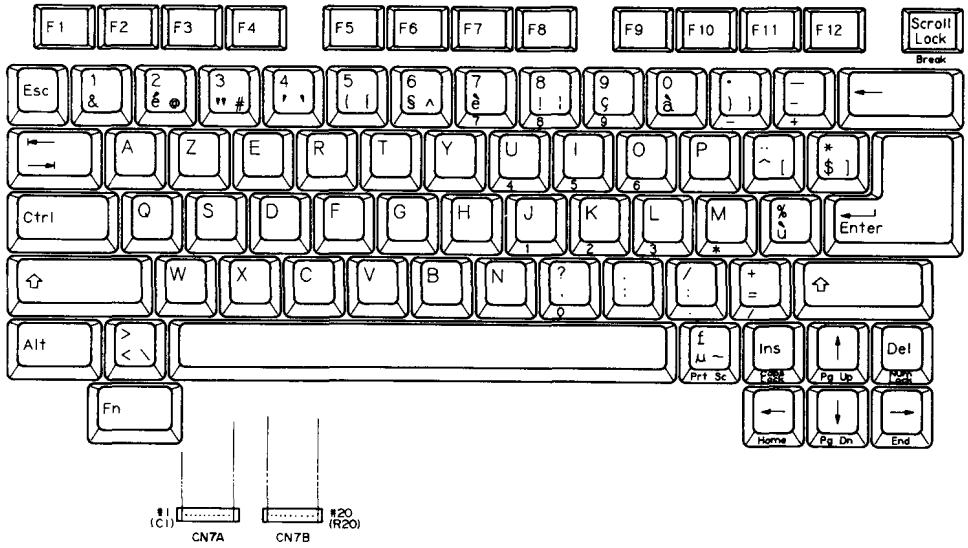
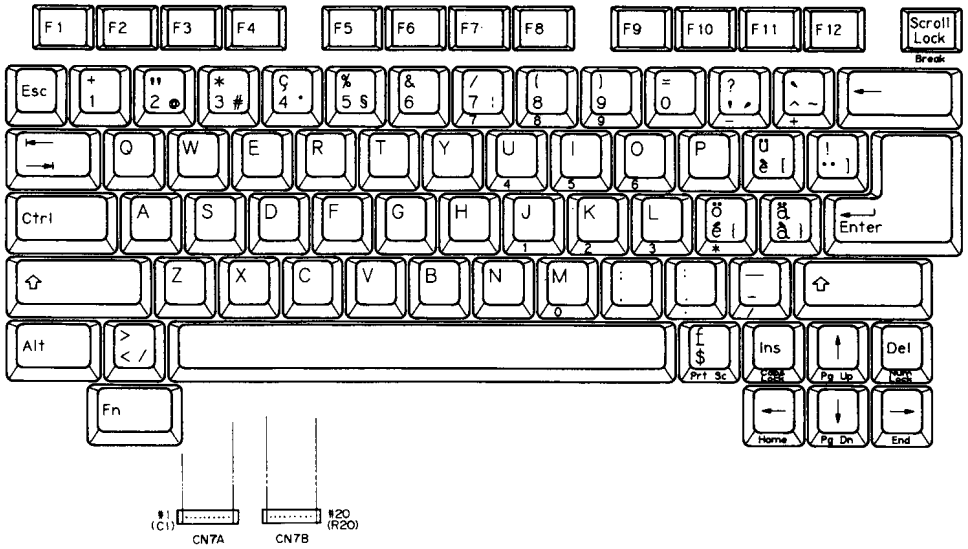
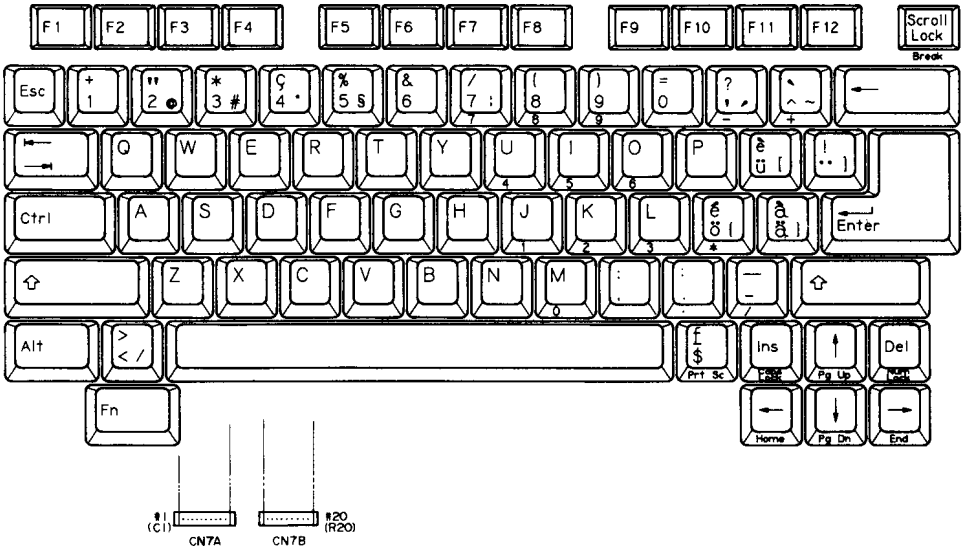


Figure 4-20. Keyboard-4 (Cont.)

Keyboard (for Swiss Roman)



Keyboard Layout (for Swiss German)



Keyboard Layout (for Germany)

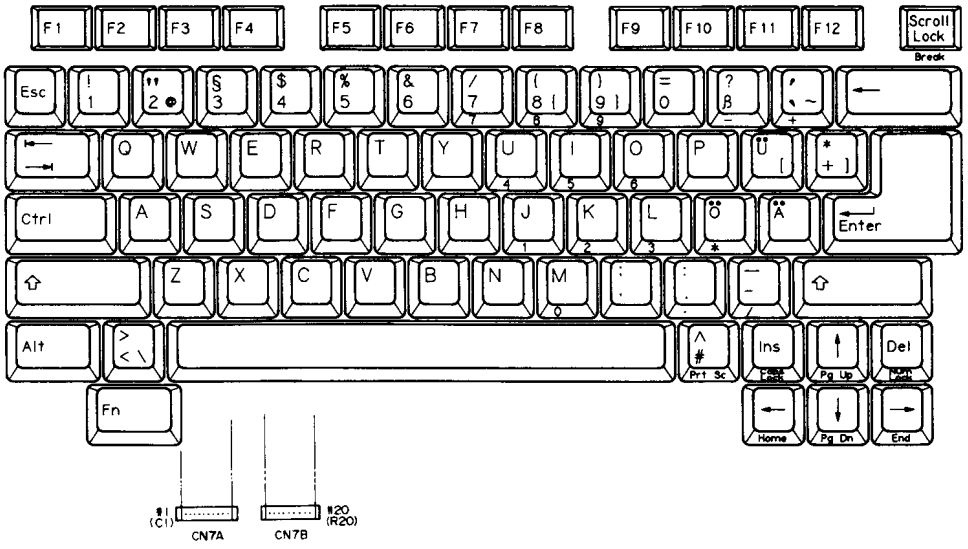
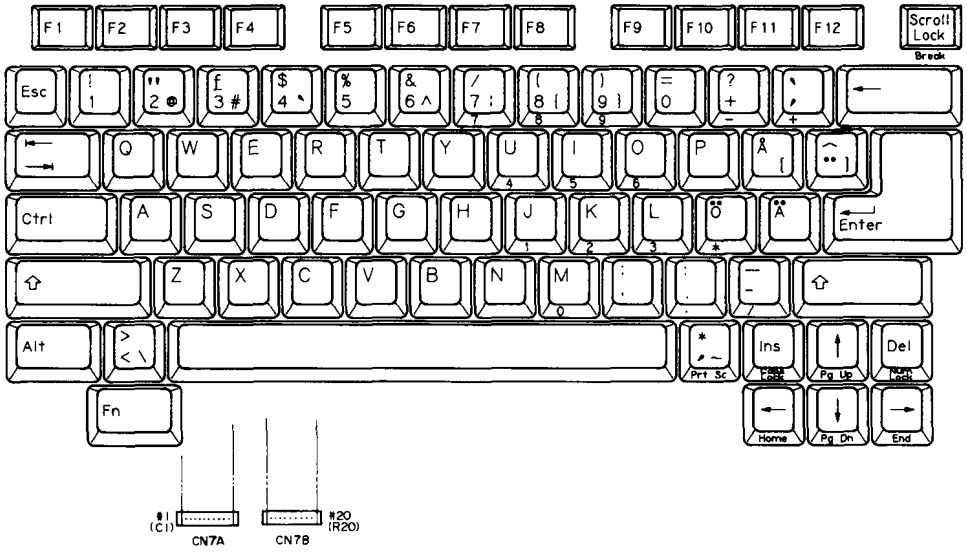
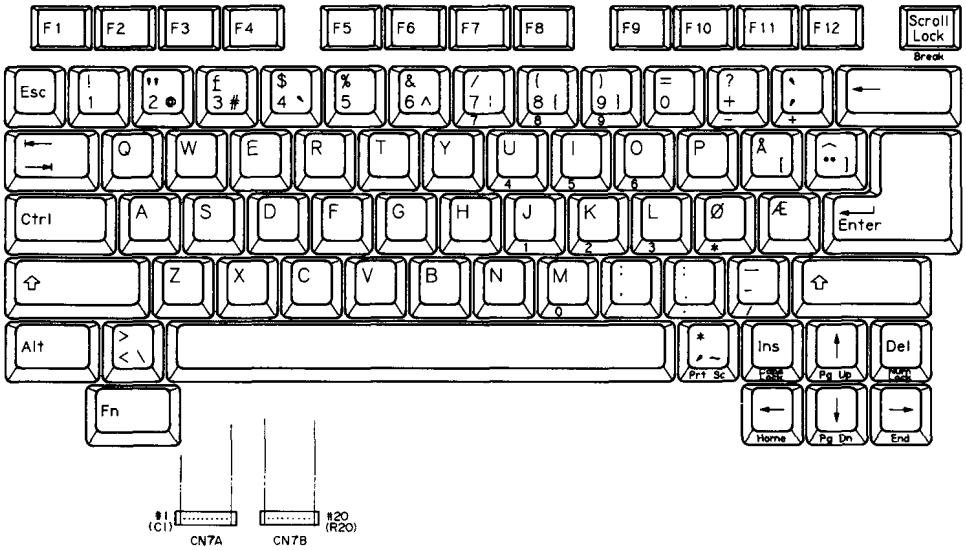


Figure 4-20. Keyboard-4 (Cont.)

Keyboard Layout (for Finland and Sweden)



Keyboard Layout (for Norway)



Keyboard Layout (for Denmark)

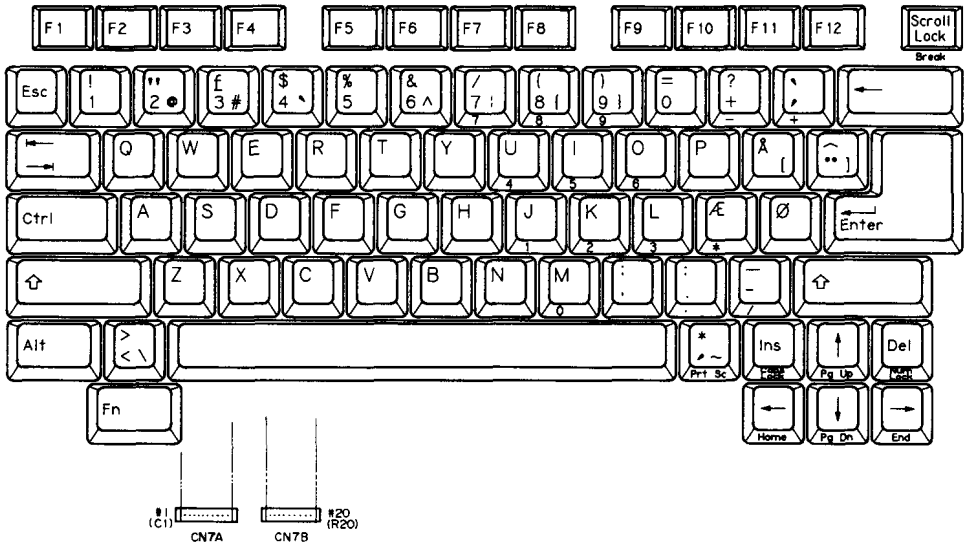


Figure 4-20. Keyboard-4 (Cont.)

Table 4-4. shows the internal keyboard scan code.

Key position	Make code in HEX	Break code in HEX
1	01	81
2	02	82
3	03	83
4	04	84
5	05	85
6	06	86
7	07	87
8	08	88
9	09	89
10	0A	8A
11	0B	8B
12	0C	8C
13	0D	8D
14	0E	8E
15	0F	8F
16	10	90
17	11	91
18	12	92
19	13	93
20	14	94
21	15	95
22	16	96
23	17	97
24	18	98
25	19	99
26	1A	9A
27	1B	9B
28	1C	9C
29	1D	9D
30	1E	9E
31	1F	9F
32	20	A0
33	21	A1
34	22	A2
35	23	A3
36	24	A4
37	25	A5
38	26	A6
39	27	A7
40	28	A8
41	2A	AA
42	2C	AC
43	2D	AD
44	2E	AE
45	2F	AF
46	30	B0
47	31	B1
48	32	B2

Table 4-4. Keyboard-1 (The Internal Keyboard Scan Code)

Key position	Make code in HEX	Break code in HEX
49	33	B3
50	34	B4
51	35	B5
52	36	B6
53	38	B8
54	2B	AB
55	39	B9
56	29/37	A9/B7
57	52/3A	D2/BA
58	48/49	C8/C9
59	53/45	D3/C5
60	4B/47	CB/C7
61	50/51	D0/D1
62	4D/4F	CD/CF
63	3B	BB
64	3C	BC
65	3D	BD
66	3E	BE
67	3F	BF
68	40	C0
69	41	C1
70	42	C2
71	43	C3
72	44	C4
73	57	D7
74	58	D8
75	46	C6
76	Nothing	Nothing

Table 4-4. Keyboard-1 (Cont.)

Example:
Key position "56"
If the "Function-key" is not held down. The "29/A9" make and break is sent.
If the "Function-key" is held down. The "37/B7" make and break is sent.
Key positions "57", "58", "59", "60", "61", and "62" have same functions.

Character Codes – Internal Keyboard

The following character codes are passed through the BIOS keyboard routine to the system or application program. The codes are returned in AL.

U.S. Keyboard Layout

MAKE CODE (Hex)	BREAK CODE (Hex)	BASE CASE (Dec)	UPPER CASE (Dec)	CTRL (Dec)	ALT (Dec)
01H	81H	ESC (27)	ESC (27)	ESC (27)	(-1)
02H	82H	1 (49)	! (33)	(-1)	Note 1
03H	83H	2 (50)	@ (64)	Note 1	Note 1
04H	84H	3 (51)	# (35)	(-1)	Note 1
05H	85H	4 (52)	$ (36)	(-1)	Note 1
06H	86H	5 (53)	% (37)	(-1)	Note 1
07H	87H	6 (54)	^ (94)	(30)	Note 1
08H	88H	7 (55)	& (38)	(-1)	Note 1
09H	89H	8 (56)	* (42)	(-1)	Note 1
0AH	8AH	9 (57)	((40)	(-1)	Note 1
0BH	8BH	0 (48)	) (41)	(-1)	Note 1
0CH	8CH	- (45)	- (95)	(31)	Note 1
0DH	8DH	= (61)	+ (43)	(-1)	Note 1
0EH BS	8EH	BS (8)	BS (8)	(127)	(-1)
0FH TAB	8FH	TAB (9)	Note 1	(-1)	(-1)
10H	90H	q (113)	Q (81)	(17)	Note 1
11H	91H	w (119)	W (87)	(23)	Note 1
12H	92H	e (101)	E (69)	(5)	Note 1
13H	93H	r (114)	R (82)	(18)	Note 1
14H	94H	t (116)	T (84)	(20)	Note 1
15H	95H	y (121)	Y (89)	(25)	Note 1
16H	96H	u (117)	U (85)	(21)	Note 1
17H	97H	i (105)	I (73)	TAB (9)	Note 1
18H	98H	o (111)	O (79)	(15)	Note 1
19H	99H	p (112)	P (80)	(16)	Note 1
1AH	9AH	[(91)	{ (123)	ESC (27)	(-1)
1BH	9BH	] (93)	} (125)	(29)	(-1)
1CH Enter	9CH	CR (13)	CR (13)	LF (10)	(-1)
1DH CTRL	9DH	(-1)	(-1)	(-1)	(-1)
1EH	9EH	a (97)	A (65)	(1)	Note 1
1FH	9FH	s (115)	S (83)	(19)	Note 1
20H	A0H	d (100)	D (68)	(4)	Note 1
21H	A1H	f (116)	F (70)	(6)	Note 1
22H	A2H	g (103)	G (71)	BEL (7)	Note 1
23H	A3H	h (104)	H (72)	BS (8)	Note 1
24H	A4H	j (106)	J (74)	LF (10)	Note 1
25H	A5H	k (107)	K (75)	(11)	Note 1
26H	A6H	l (108)	L (76)	(12)	Note 1
27H	A7H	; (59)	: (58)	(-1)	(-1)
28H	A8H	' (39)	" (34)	(-1)	(-1)
29H	A9H	` (96)	~ (126)	(-1)	(-1)
2AH SHIFT	AAH	(-1)	(-1)	(-1)	(-1)

Table 4-5. Keyboard-2 (Internal Keyboard Character Codes)

MAKE CODE (Hex)	BREAK CODE (Hex)	BASE CASE (Dec)	UPPER CASE (Dec)	CTRL (Dec)	ALT (Dec)
2BH	ABH	¥ (92)	¦ (124)	(28)	(-1)
2CH	ACH	z (122)	Z (90)	(26)	Note 1
2DH	ADH	x (120)	X (88)	(24)	Note 1
2EH	AEH	c (99)	C (67)	(3)	Note 1
2FH	AFH	v (118)	V (86)	(22)	Note 1
30H	B0H	b (98)	B (66)	(2)	Note 1
31H	B1H	n (110)	N (78)	(14)	Note 1
32H	B2H	m (109)	M (77)	CR (13)	Note 1
33H	B3H	, (44)	< (60)	(-1)	(-1)
34H	B4H	. (46)	> (62)	(-1)	(-1)
35H	B5H	/ (47)	? (63)	(-1)	(-1)
36H SHIFT	B6H	(-1)	(-1)	(-1)	(-1)
37H PrtSc	B7H	Note 3	Note 3	Note 1	(-1)
38H ALT	B8H	(-1)	(-1)	(-1)	(-1)
39H	B9H	SP (32)	SP (32)	SP (32)	SP (32)
3AH CAPS LOCK	BAH	(-1)	(-1)	(-1)	(-1)
3BH F1	BBH	Note 1	Note 1	Note 1	Note 1
3CH F2	BCH	Note 1	Note 1	Note 1	Note 1
3DH F3	BDH	Note 1	Note 1	Note 1	Note 1
3EH F4	BEH	Note 1	Note 1	Note 1	Note 1
3FH F5	BFH	Note 1	Note 1	Note 1	Note 1
40H F6	C0H	Note 1	Note 1	Note 1	Note 1
41H F7	C1H	Note 1	Note 1	Note 1	Note 1
42H F8	C2H	Note 1	Note 1	Note 1	Note 1
43H F9	C3H	Note 1	Note 1	Note 1	Note 1
44H F10	C4H	Note 1	Note 1	Note 1	Note 1
45H NUM LOCK	C5H	(-1)	(-1)	Note 2	(-1)
46H SCROLL LOCK	C6H	(-1)	(-1)	Note 2	(-1)
47H Home	C7H	Note 1	Note 1	Note 1	Note 1
48H CuUp	C8H	Note 1	Note 1	(-1)	Note 1
49H PgUp	C9H	Note 1	Note 1	Note 1	Note 1
4AH No use	CAH	(-1)	(-1)	(-1)	(-1)
4BH CuLt	CBH	Note 1	Note 1	Note 1	Note 1
4CH No use	CCH	(-1)	(-1)	(-1)	Note 1
4DH CuRt	CDH	Note 1	Note 1	Note 1	Note 1
4EH No use	CEH	(-1)	(-1)	(-1)	(-1)
4FH End	CFH	Note 1	Note 1	Note 1	Note 1
50H CuDn	D0H	Note 1	Note 1	(-1)	Note 1
51H PgDn	D1H	Note 1	Note 1	Note 1	Note 1
52H INS	D2H	Note 1,2	Note 1,2	Note 2	Note 2
53H DEL	D3H	Note 1,2	Note 1,2	Note 2	Note 2
57H F11	D7H	(-1)	(-1)	Note 2	Note 2
58H F12	D8H	(-1)	(-1)	Note 2	Note 2

Table 4-5. Keyboard-2 (Cont.)

MAKE CODE (Hex)	BREAK CODE (Hex)	BASE CASE (Dec)	UPPER CASE (Dec)	CTRL (Dec)	ALT (Dec)
08H	88H	7 (55)	7 (55)	(-1)	Note 1
09H	89H	8 (56)	8 (56)	(-1)	Note 1
0AH	8AH	9 (57)	9 (57)	(-1)	Note 1
0CH	8CH	- (45)	- (45)	(31)	Note 1
0DH	8DH	+ (43)	= (61)	(-1)	Note 1
16H	96H	4 (52)	u (117)	(21)	Note 1
17H	97H	5 (53)	i (105)	TAB (9)	Note 1
18H	98H	6 (54)	o (111)	(15)	Note 1
24H	A4H	1 (49)	j (106)	LF (10)	Note 1
25H	A5H	2 (50)	k (107)	(11)	Note 1
26H	A6H	3 (51)	l (108)	(12)	Note 1
27H	A7H	* (42)	; (59)	(-1)	(-1)
32H	B2H	0 (48)	m (109)	CR (13)	Note 1
34H	B4H	. (46)	. (46)	(-1)	(-1)
35H	B5H	/ (47)	/ (47)	(-1)	(-1)

Table 4-5. Keyboard-2 (Cont.)

NOTE 1 Refer to Extended Codes.
2 Refer to Special Handling.
3 Pressing the PRINT SCREEN (Key 37H) will result in an interrupt invoking the print screen routine.

Keyboard Extended Functions

SECOND CODE (Hex)	FUNCTION
03H	NUL Character
0FH	Back Tab
10H-19H	ALT Q,W,E,R,T,Y,U,I,O,P
1EH-26H	ALT A,S,D,F,G,H,J,K,L
2CH-32H	ALT Z,X,C,V,B,N,M
3BH-44H	F1-F10 Function Keys Base Case
47H	Home
48H	Cursor Up
49H	Page Up & Home Cursor
4BH	Cursor Left
4DH	Cursor Right
4FH	End
50H	Cursor Down
51H	Page Down & Home Cursor
52H	INS
53H	DEL
54H-5DH	F11-F20 (Upper Case F1-F10)
5EH-67H	F21-F30 (CTRL F1-F10)
68H-71H	F31-F40 (ALT F1-F10)
72H	CTRL PRTSC (Start/Stop Echo to Printer)
73H	CTRL Cursor Left (Reverse Word)
74H	CTRL Cursor Right (Advance Word)
75H	CTRL End (Erase EOL)
76H	CTRL Page Down (Erase EOS)
77H	CTRL Home (Clear Screen and Home)
78H-83H	ALT 1,2,3,4,5,6,7,8,9,0,-,=
84H	CTRL Page Up (Top 25 Lines of Text & Home Cursor)

Table 4-6. Keyboard-3 (Extended Codes)

For certain functions that cannot be represented in the standard ASCII codes, an extended code is used. NUL code (a character code of 00) is returned in AL. This indicates that the system or application program should examine a second code that will indicate the actual function. Usually, but not always, this second code is the scan code of the primary key that was pressed. This code is returned in AH.

Special Handling

1. System Reset
   The combination of ALT-CTRL-DEL will result in the keyboard routine initiating the equivalent of a system reset/reboot.

2. System Set Up
   The combination of ALT-CTRL-INS will result in the keyboard routine displaying the system default values. In relation to CRT or LCD selection, the combinations of ALT-CTRL-F11 (CRT) and ALT-CTRL-F12 (LCD) will be valid.
   NOTE: To press F11 and F12 keys are not equal to press SHIFT F1 and F2.

3. Break
   The combination of CTRL SCROLL-LOCK will result in the keyboard routine signaling interrupt-1A. Also, the extended characters (AL = 00H, AH = 00H) will be returned.
   NOTE: It is up to the system or application initialization code to change the interrupt vector in order to support an actual "break" function.

4. Pause
   The combination of CTRL NUM-LOCK will cause the keyboard interrupt routine to loop, waiting for any key except NUM-LOCK to be pressed.

IV-13. External Keyboard

Communication Protocol

The External keyboard shall communicate with the system using synchronus serial protocol. When no communication is in process, the keyboard holds the data line Low and the clock line High. Transmissions consist of a 10 bit data word.

Keyboard RTS	Start	B0	B1	B2	B3	B4	B5	B6	B7
0	1	*	*	*	*	*	*	*	*

The system may hold the clock line low for a minimum of 12.5msec to initiate a keyboard reset. The External keyboard shall not attempt to tramsmit data while the clock line is being held by the system. Before initiating a transmission, the External keyboard lowers the clock line as a RTS (Request To Send). The External Keyboard then checks the state of the data line. If the system is holding the data line low, then the External keyboard interface is inhibited. The External keyboard shall return the keycode in the buffer, return the clock and data lines to idle state and resume scanning until the interface is enabled. If the interface is enabled, the External keyboard shall transmit its data. Data is valid during the falling edge of the clock. Figure 4-21 shows the External keyboard interface circuit and timing diagram.

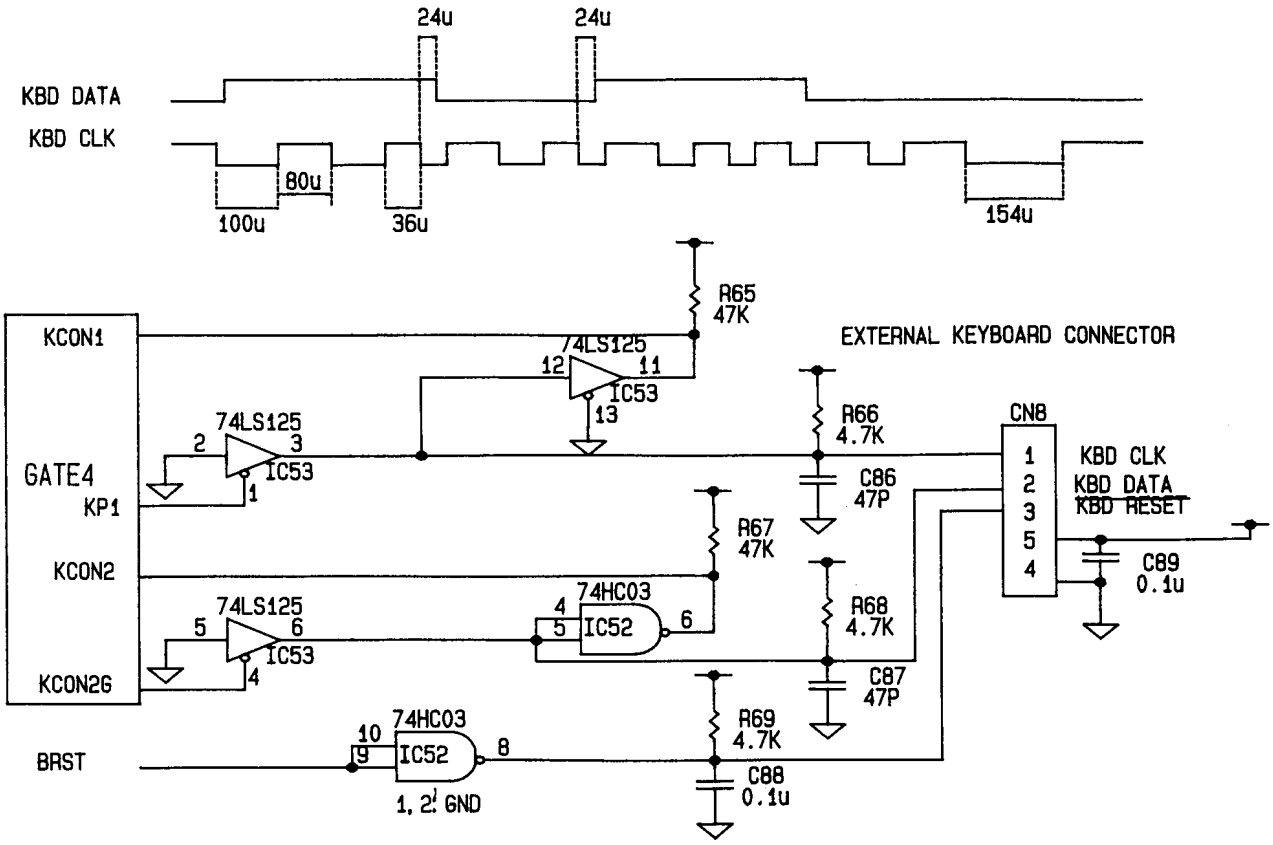


Figure 4-21. Keyboard-5 (The External Keyboard Interface Circuit and Timing Diagram)

Character Codes – Enhanced Keyboard

The following character codes are passed through the BIOS keyboard routine to the system or application program. The codes are returned in AL.

U.S. Keyboard Layout

MAKE CODE (Hex)	BREAK CODE (Hex)	BASE CASE (Dec)	UPPER CASE (Dec)	CTRL (Dec)	ALT (Dec)
01H	81H	ESC (27)	ESC (27)	ESC (27)	(-1)
02H	82H	1 (49)	! (33)	(-1)	Note 1
03H	83H	2 (50)	@ (64)	Note 1	Note 1
04H	84H	3 (51)	# (35)	(-1)	Note 1
05H	85H	4 (52)	$ (36)	(-1)	Note 1
06H	86H	5 (53)	% (37)	(-1)	Note 1
07H	87H	6 (54)	^ (94)	(30)	Note 1
08H	88H	7 (55)	& (38)	(-1)	Note 1
09H	89H	8 (56)	* (42)	(-1)	Note 1
0AH	8AH	9 (57)	((40)	(-1)	Note 1
0BH	8BH	0 (48)	) (41)	(-1)	Note 1
0CH	8CH	- (45)	- (95)	(31)	Note 1
0DH	8DH	= (61)	+ (43)	(-1)	Note 1
0EH BS	8EH	BS (8)	BS (8)	(127)	(-1)
0FH TAB	8FH	TAB (9)	Note 1	(-1)	(-1)
10H	90H	q (113)	Q (81)	(17)	Note 1
11H	91H	w (119)	W (87)	(23)	Note 1
12H	92H	e (101)	E (69)	(5)	Note 1
13H	93H	r (114)	R (82)	(18)	Note 1
14H	94H	t (116)	T (84)	(20)	Note 1
15H	95H	y (121)	Y (89)	(25)	Note 1
16H	96H	u (117)	U (85)	(21)	Note 1
17H	97H	i (105)	I (73)	TAB (9)	Note 1
18H	98H	o (111)	O (79)	(15)	Note 1
19H	99H	p (112)	P (80)	(16)	Note 1
1AH	9AH	[(91)	{ (123)	ESC (27)	(-1)
1BH	9BH	] (93)	} (125)	(29)	(-1)
1CH Enter	9CH	CR (13)	CR (13)	LF (10)	(-1)
1DH CTRL	9DH	(-1)	(-1)	(-1)	(-1)
1EH	9EH	a (97)	A (65)	(1)	Note 1
1FH	9FH	s (115)	S (83)	(19)	Note 1
20H	A0H	d (100)	D (68)	(4)	Note 1
21H	A1H	f (116)	F (70)	(6)	Note 1
22H	A2H	g (103)	G (71)	BEL (7)	Note 1
23H	A3H	h (104)	H (72)	BS (8)	Note 1
24H	A4H	j (106)	J (74)	LF (10)	Note 1
25H	A5H	k (107)	K (75)	(11)	Note 1
26H	A6H	l (108)	L (76)	(12)	Note 1
27H	A7H	; (59)	: (58)	(-1)	(-1)
28H	A8H	' (39)	" (34)	(-1)	(-1)
29H	A9H	` (96)	~ (126)	(-1)	(-1)
2AH SHIFT	AAH	(-1)	(-1)	(-1)	(-1)
2BH	ABH	¥ (92)	| (124)	(28)	(-1)

Table 4-7. Keyboard-4 (Enhanced Keyboard Character Codes)

MAKE CODE (Hex)	BREAK CODE (Hex)	BASE CASE (Dec)	UPPER CASE (Dec)	CTRL (Dec)	ALT (Dec)
2CH	ACH	z (122)	Z (90)	(26)	Note 1
2DH	ADH	x (120)	X (88)	(24)	Note 1
2EH	AEH	c (99)	C (67)	(3)	Note 1
2FH	AFH	v (118)	V (86)	(22)	Note 1
30H	B0H	b (98)	B (66)	(2)	Note 1
31H	B1H	n (110)	N (78)	(14)	Note 1
32H	B2H	m (109)	M (77)	CR (13)	Note 1
33H	B3H	, (44)	< (60)	(-1)	(-1)
34H	B4H	. (46)	> (62)	(-1)	(-1)
35H	B5H	/ (47)	? (63)	(-1)	(-1)
36H SHIFT	B6H	(-1)	(-1)	(-1)	(-1)
37H PrtSc	B7H	* (42)	Note 3	Note 1	(-1)
38H ALT	B8H	(-1)	(-1)	(-1)	(-1)
39H	B9H	SP (32)	SP (32)	SP (32)	SP (32)
3AH CAPS LOCK	BAH	(-1)	(-1)	(-1)	(-1)
3BH F1	BBH	Note 1	Note 1	Note 1	Note 1
3CH F2	BCH	Note 1	Note 1	Note 1	Note 1
3DH F3	BDH	Note 1	Note 1	Note 1	Note 1
3EH F4	BEH	Note 1	Note 1	Note 1	Note 1
3FH F5	BFH	Note 1	Note 1	Note 1	Note 1
40H F6	C0H	Note 1	Note 1	Note 1	Note 1
41H F7	C1H	Note 1	Note 1	Note 1	Note 1
42H F8	C2H	Note 1	Note 1	Note 1	Note 1
43H F9	C3H	Note 1	Note 1	Note 1	Note 1
44H F10	C4H	Note 1	Note 1	Note 1	Note 1
45H NUM LOCK	C5H	(-1)	(-1)	Note 2	(-1)
46H SCROLL LOCK	C6H	(-1)	(-1)	Note 2	(-1)
57H F11	D7H	(-1)	(-1)	Note 2	Note 2
58H F12	D8H	(-1)	(-1)	Note 2	Note 2

Table 4-7. Keyboard-4 (Cont.)

MAKE CODE (Hex)	BREAK CODE (Hex)	BASE CASE (Dec)	UPPER CASE (Dec)	CTRL (Dec)	ALT (Dec)
47H Home	C7H	7 (55)	Note 1	Note 1	Note 1
48H CuUp	C8H	8 (56)	Note 1	(-1)	Note 1
49H PgUp	C9H	9 (57)	Note 1	Note 1	Note 1
4AH	CAH	- (45)	- (45)	(-1)	(-1)
4BH CuLt	CBH	4 (52)	Note 1	Note 1	Note 1
4CH	CCH	5 (53)	(-1)	(-1)	Note 1
4DH CuRt	CDH	6 (54)	Note 1	Note 1	Note 1
4EH	CEH	+ (43)	+ (43)	(-1)	(-1)
4FH End	CFH	1 (49)	Note 1	Note 1	Note 1
50H CuDn	D0H	2 (50)	Note 1	(-1)	Note 1
51H PgDn	D1H	3 (51)	Note 1	Note 1	Note 1
52H INS	D2H	0 (48)	Note 1,2	Note 2	Note 2
53H DEL	D3H	. (46)	Note 1,2	Note 2	Note 2

Table 4-8. Keyboard-5 (Numeric Lock States)

NOTE: 1 Refer to Extended Codes.
2 Refer to Special Handling.
3 Pressing the PRINT SCREEN (Key 37H) will result in an interrupt invoking the print screen routine.

IV-14. Floppy Disk Drive

FDD PERIPHERAL CIRCUITRY

The TANDY 1400LT is equiped with two 3.5 inch floppy disk drives. And one External 5.25inch FDD can be connected. (However, to connect the external FDD, an extra power supply is required.)

Figure 4-22 shows the FDD and peripheral circuitry block diagram.

The TANDY 1400LT uses μPD72065C. For floppy disk controller and SED9420CAC for VFO. Data transmission from the FDD is performed in the DMA mode and is controlled by 82C37

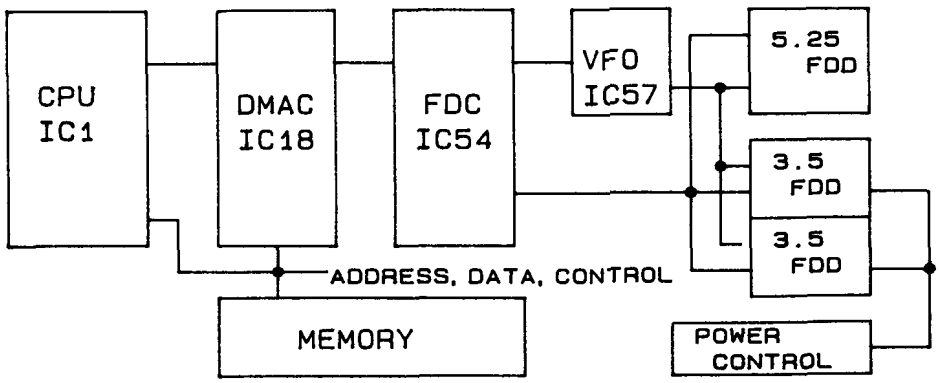


Figure 4-22. The FDD and Peripheral Circuitry Block Diagram

DMA operation

A DMA request (DR2) is generated by the FDC (IC54). After receiving the DMA request, the DMA controller (IC18) will issue a Hold request (HDA signal) to the host CPU. The system buses are not released to the DMA controller until a Hold Acknowlege signal (HLA signal) is returned to the DMA controller from the CPU. After the Hold Acknowledge has been received, address and control signals are generated by the DMA controller to accomplish the DMA transfers.

Data is transfered directly from the FDC to memory (or vice versa) with "0" active BIR, BIW, BMR, and BMW being active.

In advance, the segment address is set to the GATE4, and in DMA cycle the GATE4 encodes DMA Acknowledge signal, and it outputs address of permitting DMA channel to A16 - A19 bus.

DMA Control

All data transmissions between FDC and the CPU performed in the DMA mode. Figure 4-23 shows the DMA controller and peripheral circuitry.

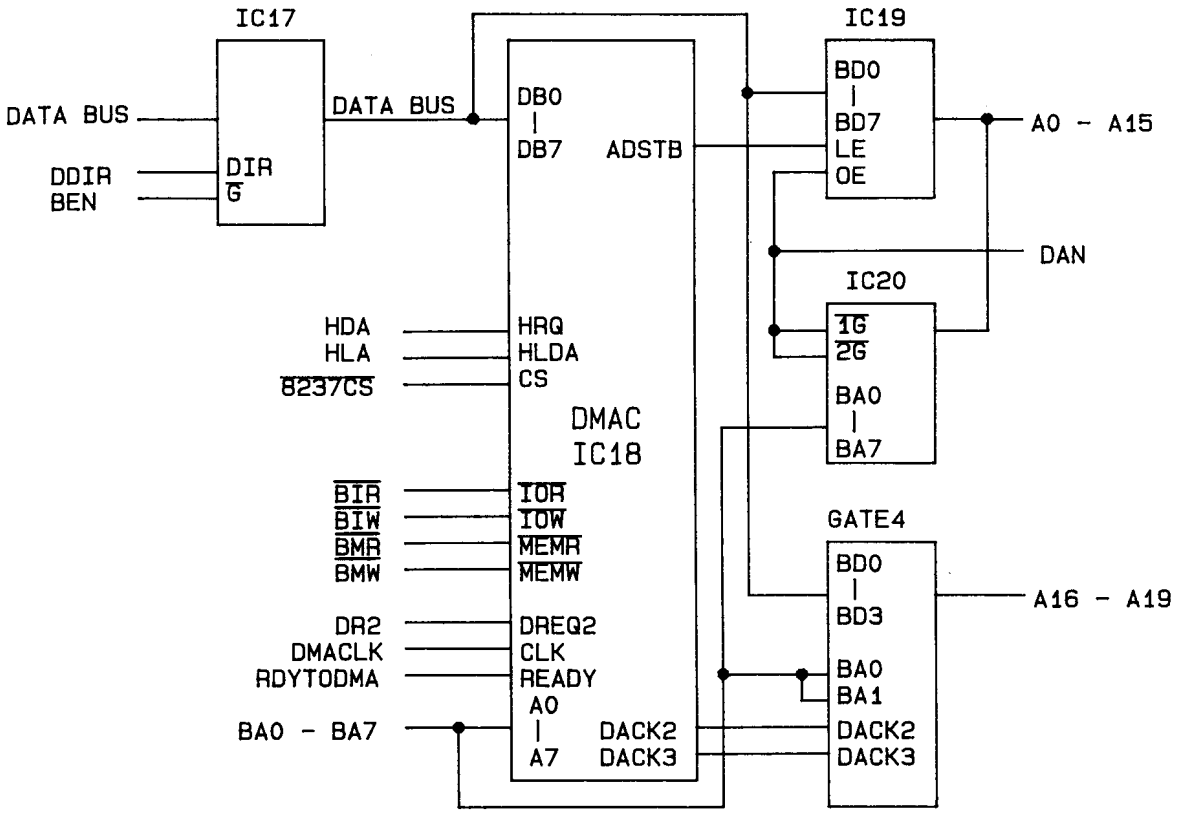


Figure 4-23. DMA Controller and Peripheral Circuitry

FDD Control

CPU INTERFACE

Figure 4-24 shows the CPU interface for FDC. The clock for FDC is supplied from VFO (4MHz clock). The reset signal (RESET765) is fed to the reset terminal. The terminal A0 selects the contents to be sent to the data bus. When it is set, the data register contents are sent, when it is reset, the status register are sent. "0" active signals IR (IW) input allows the transfer of data from (to) the FDC to (from) the data bus. The FDC is selected when "$\overline{\text{CS765}}$" is low, enabling IR, IW and A0.

The FDC sets the INT terminal to HIGH when the command is executed.

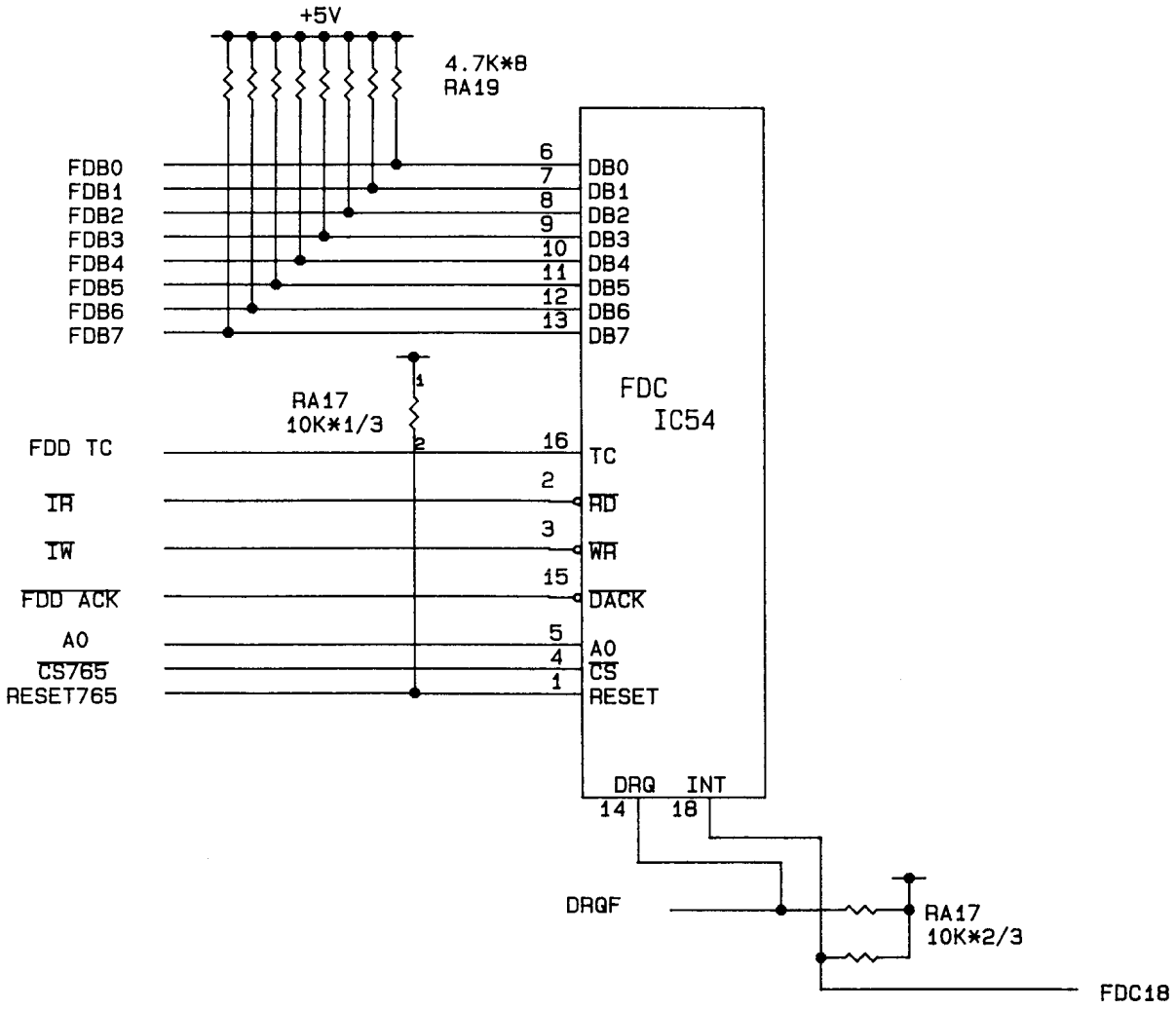


Figure 4-24. CPU Interface for FDC

FDD INTERFACE

Figure 4-25 shows the FDD interface circuitry.

Signal for FDD : "LOW" active $\overline{\text{DRIVE SEL0-2 (3.5)}}$, $\overline{\text{MOTOR ENA (3.5)}}$, "HIGH" active DRIVE SEL0,2 (5.25), MOTOR ENA (5.25) are latched in the GATE5. These are set by the I/O system command. The FDD control signal for External 5.25 inch disk is driven by 74ALS240. The FDD control signal for the input system is pulled up by the resistor. The External FDD (5.25) control signal and input signal for system are terminated by the capacitor.

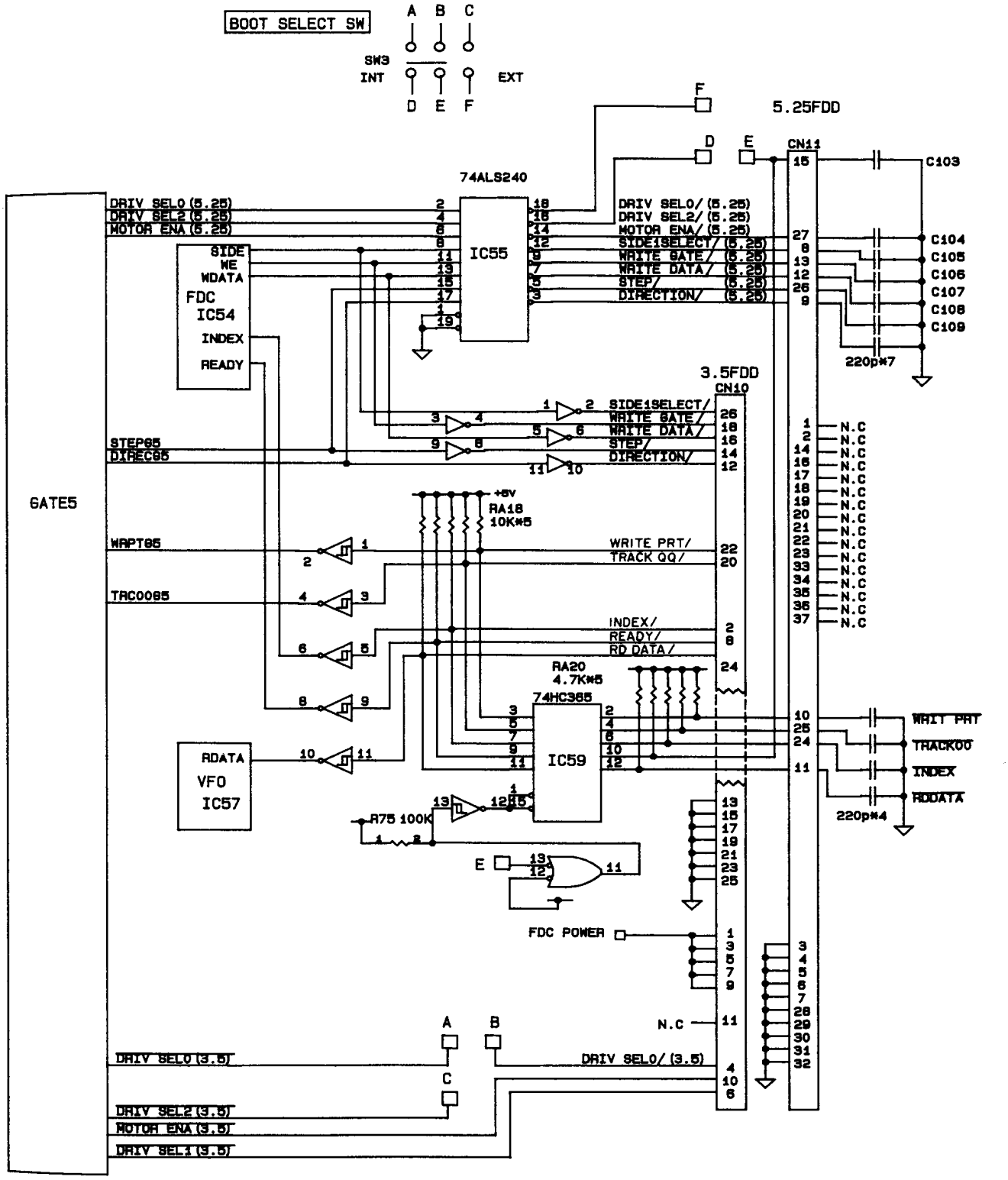


Figure 4-25. FDD Interface Circuitry

The drive assignment is switchable by the BOOT SELECT Switch (SW3)
The following are drive assignments.

	3.5 inch boot	5.25 inch boot
DRIVE 1	DRIVE A	DRIVE C
DRIVE 2	DRIVE B	DRIVE B
EXT FDD	DRIVE C	DRIVE A

VFO (DATA SEPARATOR FOR FDD)

The VFO (IC57) is a CMOS VFO data separator for use in the floppy disk interface. The VFO removes bit phase shift origination in variations in disk rotation speed or peak shifts from disk drive read data to generate data window and reproduces read data pulse signals for output to a floppy disk controller. It provides the following outputs as FDC clocks. CLK1: 4MHz, WCLK (Write clock): 5.25 inch MFM Interval T = 2usec.
Figure 4-26 shows VFO and FDC interface.

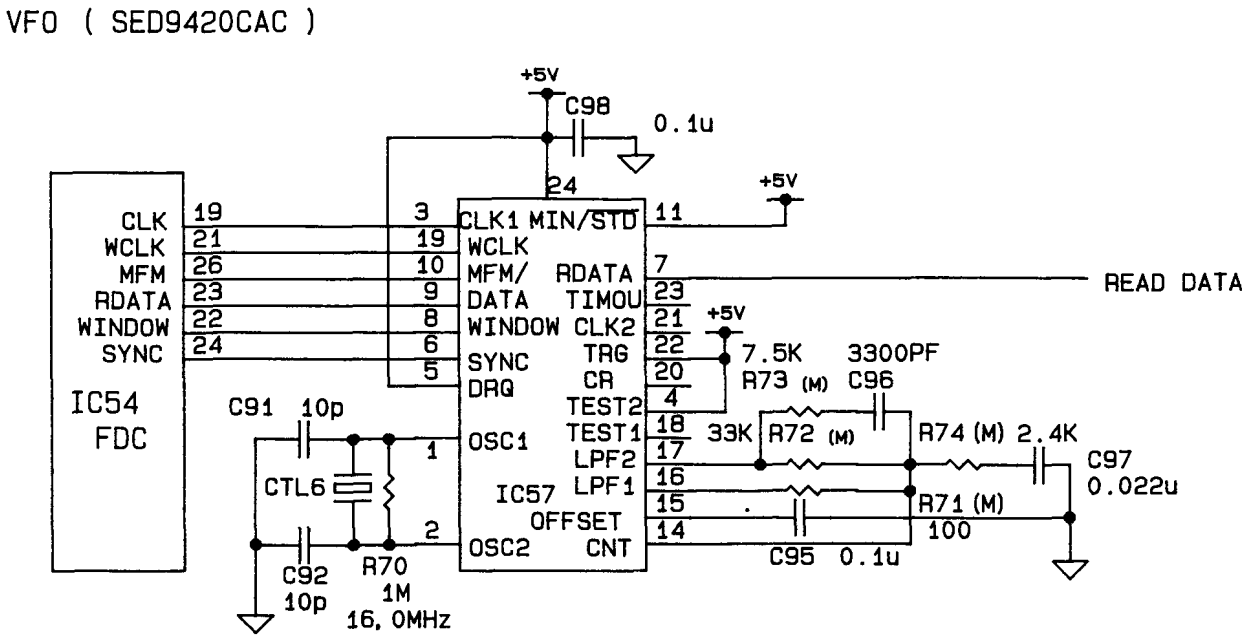


Figure 4-26. VFO and FDC Interface

External FDD connector is DB - 37-pin female type.
Table 4-15 shows the External FDD connector pin assignments.

PIN NUMBER	CONTENTS
1	NC
2	NC
3-7	Ground
8	BSIDESE*
9	CDIR*
10	WRPRT*
11	RDDATA*
12	WRDATA*
13	WEN*
14	NC
15	DSEXT*
16-23	NC
24	INDEX*
25	TRKO*
26	STEP*
27	BMTRON*
28-32	Ground
33-37	NC

Table 4-9. External FDD Connector Pin Assignments

IV-15. Printer Interface

Figure 4-27 shows printer interface circuit.

The Command of printer or data is loaded to 8 bit latched output port, and the "0" active STROBE signal line is activated writing data to the printer. The printer interface program then reads the status pins of printer ports to see if the next character can be sent, if the printer is ready, the program activates the IRQ7, indicating printer is not musy to the system program.

Printer control I/O's are 378H, 379H and 37AH.

Figure 4-28 shows timing diagram between CPU and Printer.

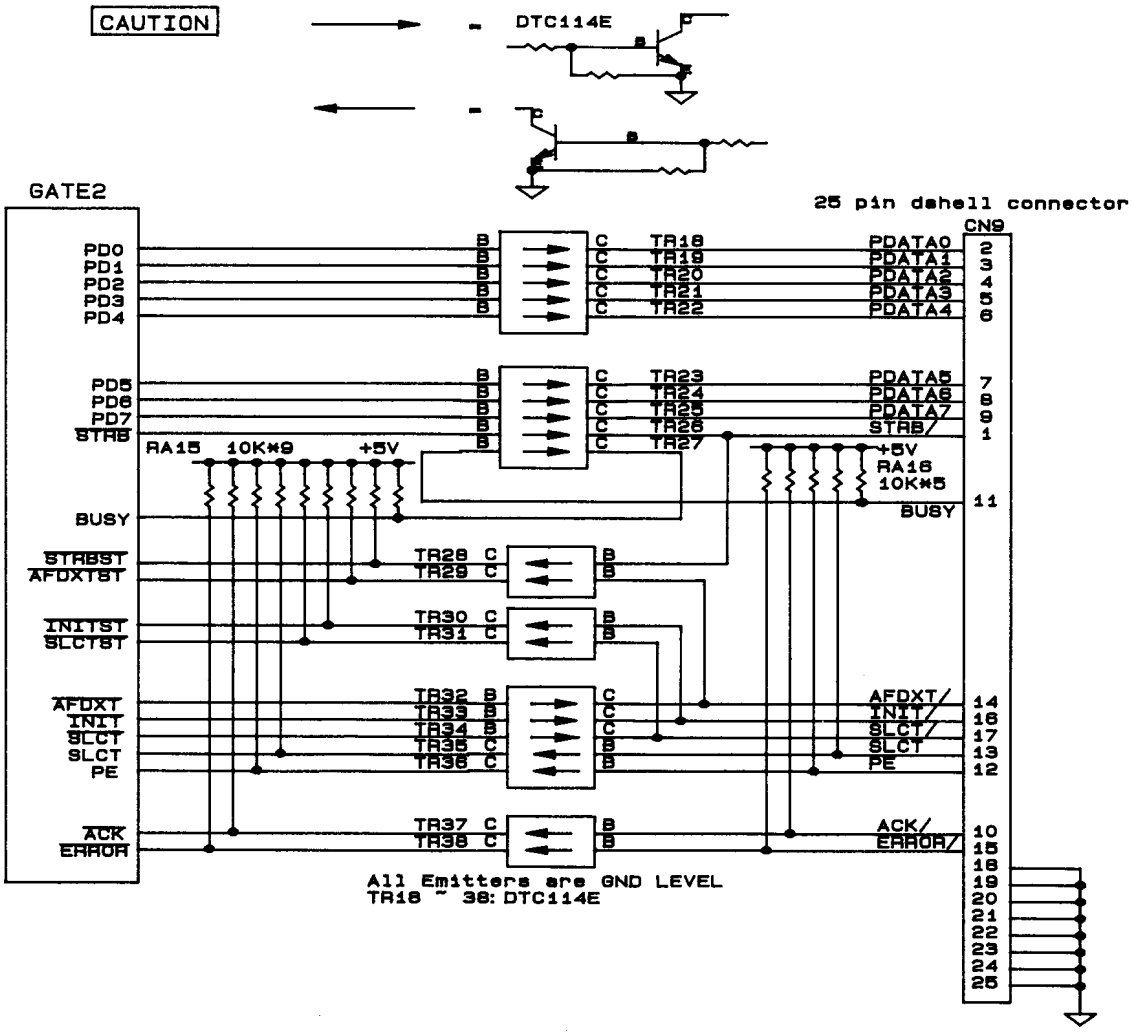


Figure 4-27. Printer Interface Circuit

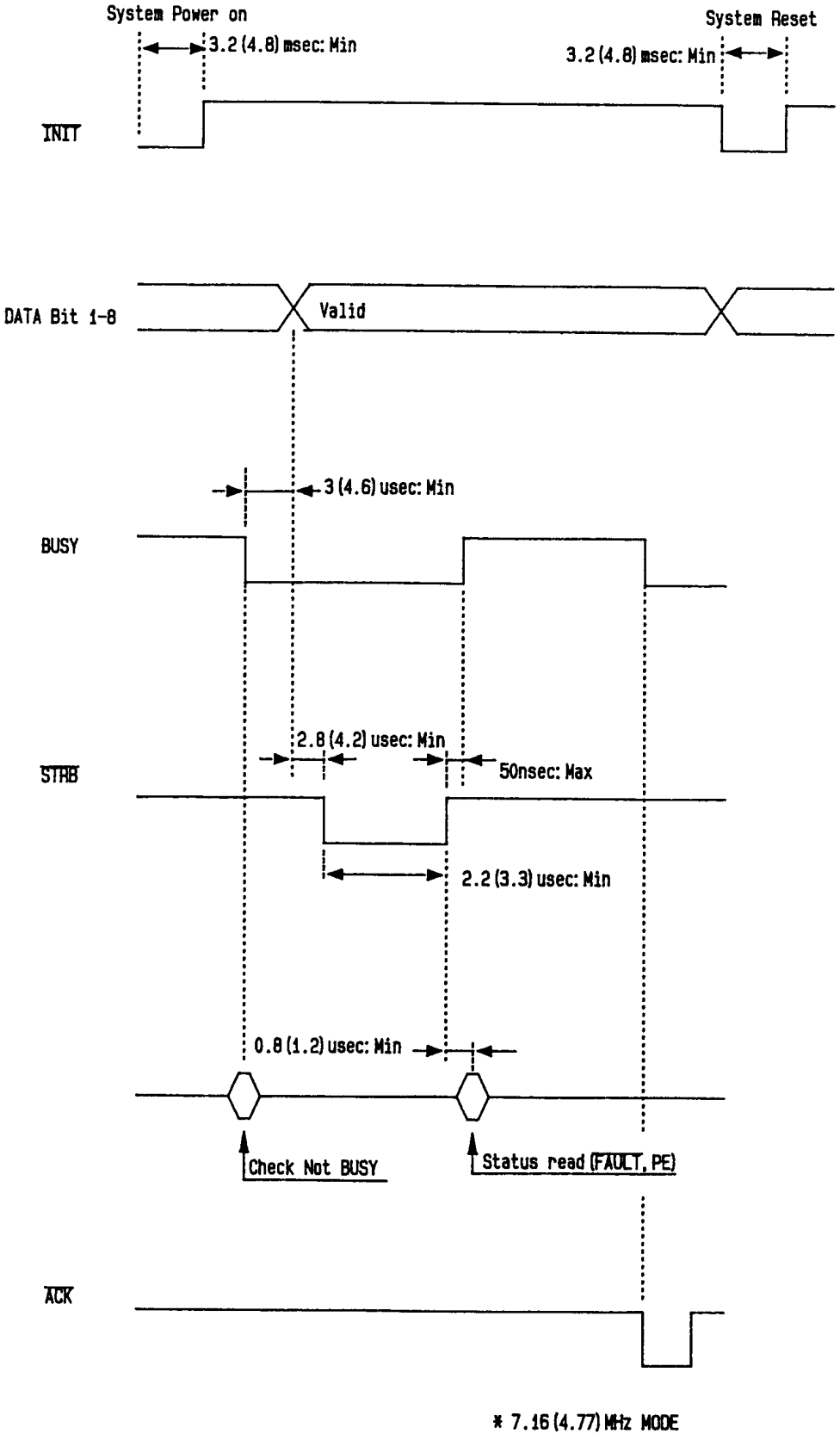


Figure 4-28. Timing Diagram between CPU and Printer

IV-16. LCD Controller

This LCD controller supports three display devices.

1. LCD pannel.
2. CRT with IRGB input.
3. CRT with COMPOSITE input.

This LCD controller is compatible with the color adapter for IBM-PC.

CPU Interface

The CPU interface circuit of the V6355 is shown in Figure 4-29.

Data Bus (D0 - D7), $\overline{\text{IOSEL}}$ (Chip select signal), $\overline{\text{MEMSEL}}$ (VRAM chip select signal), $\overline{\text{IOW}}$ (I/O write signal), $\overline{\text{IOR}}$ (I/O read signal), MEMRDY (Memory request signal), and Address Bus (A0 - A3) serve as the interface between the CPU and the V6355.

The addressing to all I/O registers is executed by the I/O command of the four least significant bits (A0 - A3)of port addresses with a "Low" active $\overline{\text{IOSEL}}$ signal, which enables this controller like chip selecting.

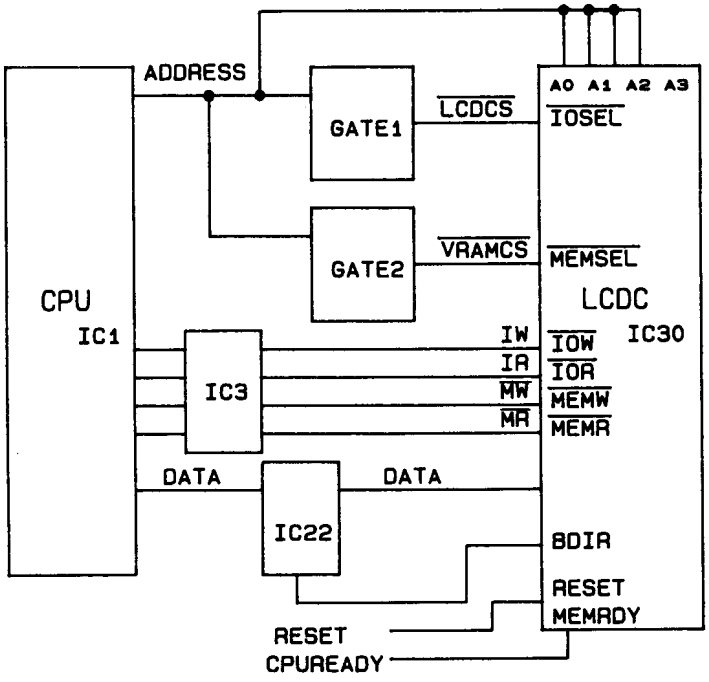


Figure 4-29. LCDC-CPU Interface

VRAM - CPU Interface

The TANDY 1400LT uses two 8K byte static RAMs (total 16K byte) for the VIDEO RAM. This memory contains 640 × 200 dots data for graphic display.

The CPU can access it anytime without display flicker.

The VIDEO RAM can be accessed completely in the same way as accessing normal memory RAM from the CPU. Write and Read functions are freely executed without checking the status of the display control device.

This controller will be selected by "0" active $\overline{\text{MEMSEL}}$ (VRAM chip select signal), and "0" active $\overline{\text{MEMW}}$ (MEMORY write signal) or $\overline{\text{MEMR}}$ (MEMORY read signal).

Figure 4-30 shows VRAM-LCDC interface.

The timing chart is shown in Figure 4-31.

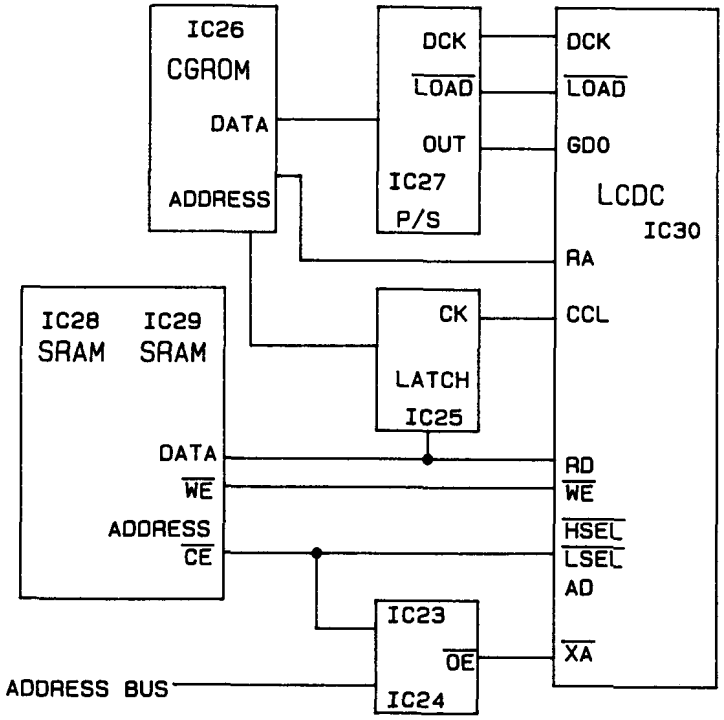


Figure 4-30. VRAM-LCDC Interface

Parameter	Symbol	Minimum	Maximum	Unit
Read/Write High-Level Pulse Width	PW_H	50		ns
Read/Write Rise and Fall Time	t_r, t_f		25	ns
Address Setup Time	t_{AS}	0		ns
Address Hold Time	t_{AH}	0		ns
Data Delay Time (During Write)	t_{DW}		350	ns
Data Hold Time (During Write)	t_{HW}	0		ns
Data Setup Time (During Read)	t_{DS}	0		ns
Data Hold Time (During Read)	t_{HR}	10		ns
Bus Direction Switching Delay Time	t_{BD}		80	ns
Bus Direction Switching Hold Time	t_{BH}	10		ns
Read - Low-Level Delay Time	t_{RD}		80	ns
Read - High-Level Hold Time	t_{RH}	10		ns
Read - Rise Time	t_{Rr}		50	ns

@CL = 100 pF + 2LSTTL (CD0 to CD7, BDIR, MEMRDY)

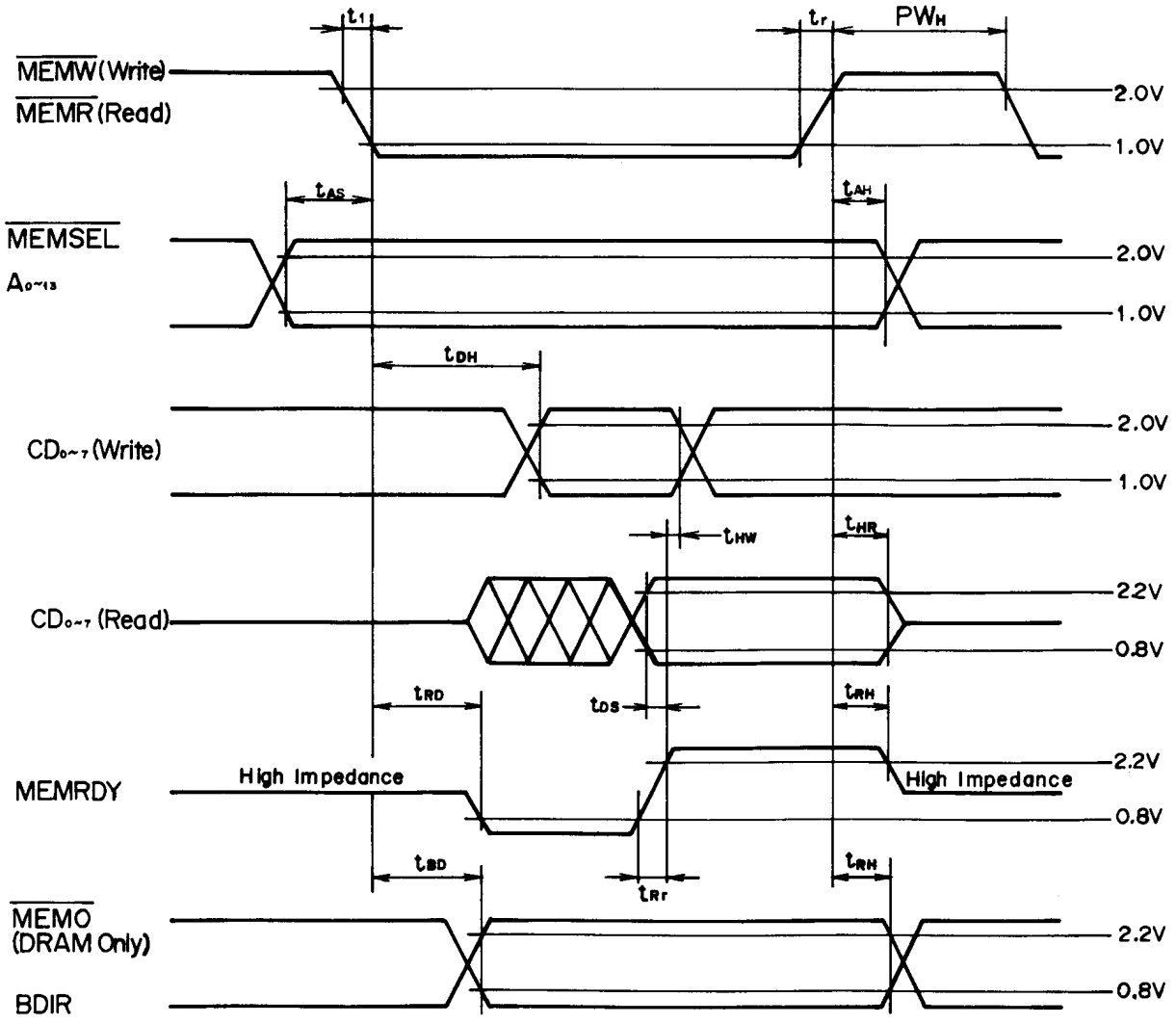


Figure 4-31. VRAM-LCDC Timing Chart

LCD Unit Interface

The interface signal between LCD controller and LCD Unit is shown in Figure 4-32.

Signal	Function
UD0 - 3	Data input signal for displaying at upper half area of LCD. "High" level - White color, "Low" level - Black color.
LD0 - 3	Data input signal for displaying at lower half area of LCD. "High" level - White color, "Low" level - Black color.
CLP	The shift clock signal of display data. The display data (UD0 - UD3 and LD0 - LD3) is input at the falling edge of this signal.
LIP	Signal for latching 1 line shift register. DATA & common driver DATA shift signal.
FRP	Start signal of each display cycle (Shift register DATA signal of common driver.)
FRMB	A.C signal for LCD driving.
CE0	Chip-enable clock pulse of segment driver IC.

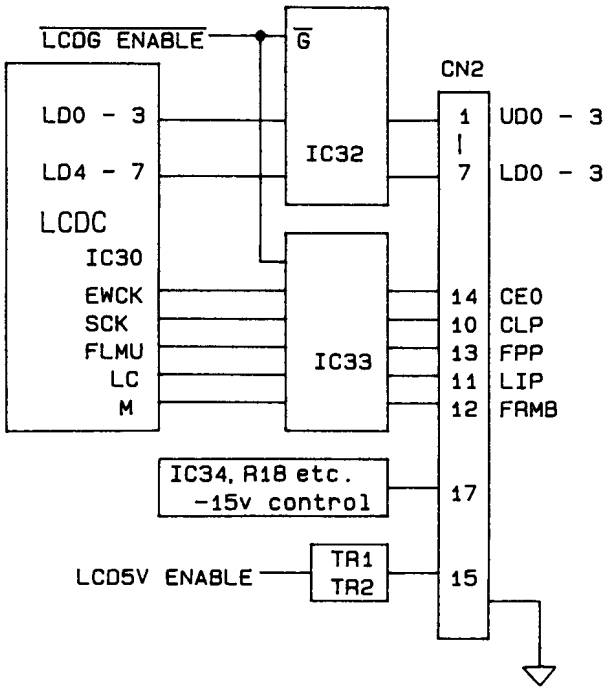


Figure 4-32. Interface Signal between LCDC and LCD unit

Figure 4-33 shows LCD interface timing diagram.

Typ2 Mode

Parameter	Symbol	Min.	Typical	Max.	Unit
FLM - LC Setup Time	t_{FLS}	320			ns
FLM - LC Hold Time	t_{FLH}	320			ns
LC High-Level Pulse Width	t_{LH}	320			ns
LC - SCK Delay Time	t_{LSD}	8			μs
SCK - LC Delay Time	t_{SLD}	500			ns
Data - SCK Setup Time	t_{DSS}	140			ns
Data - SCK Hold Time	t_{DSH}	140			ns
LC, SCK and EWCK Rise and Fall Times	t_r, t_f			50	ns
SCK High-Level Pulse Width	t_{SH}	320			ns
SCK Low-Level Pulse Width	t_{SL}	320			ns
SCK Cycle Time	t_{SC}	740			ns
EWCK Setup Time	t_{ES}	140			ns
EWCK Hold Time	t_{EH}	140			ns
EWCK High-Level Pulse Width	t_{EWH}	140			ns
M Delay Time	t_D			50	ns

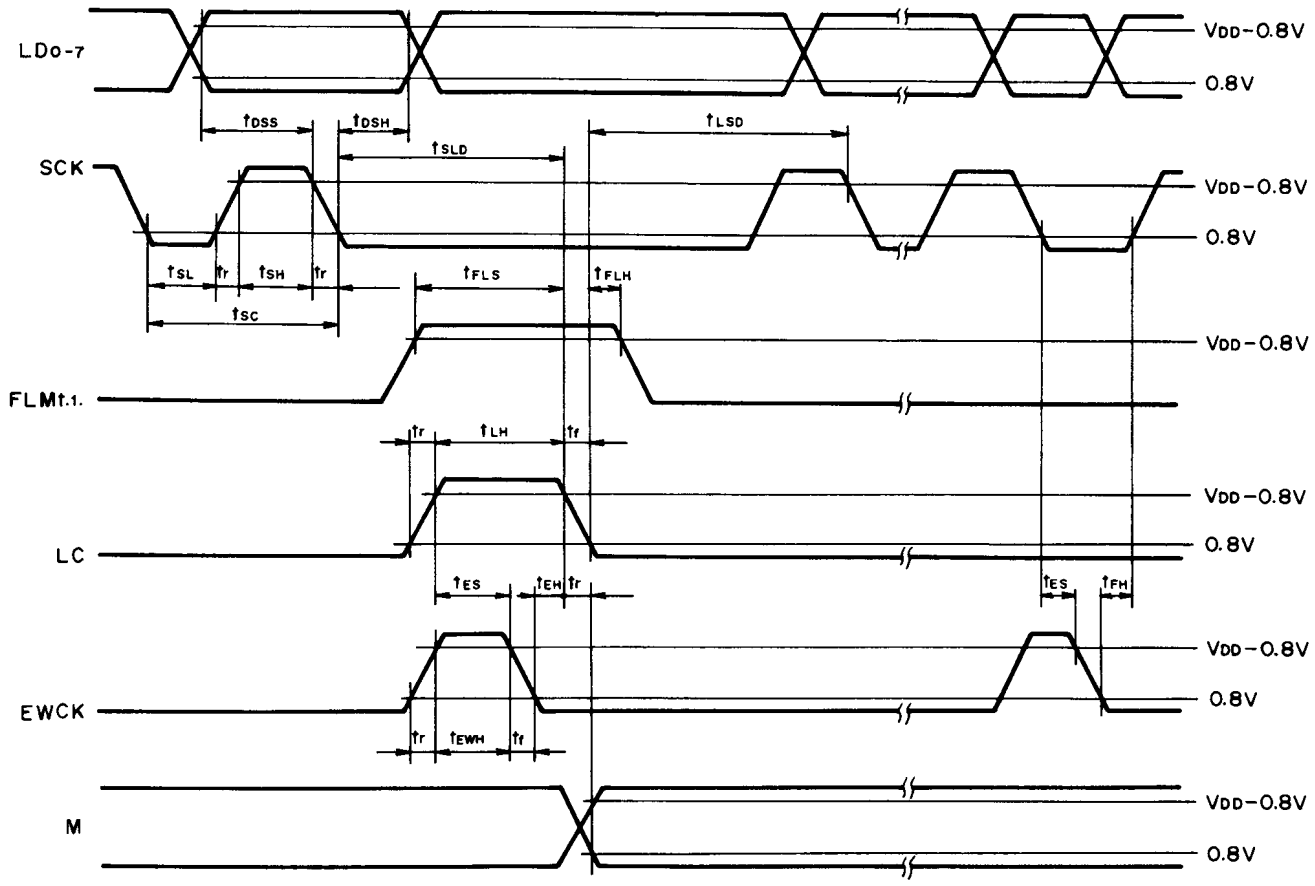


Figure 4-33. LCD Interface Timing Diagram

NTSC composite and IRGB Interface

Figure 4-34 shows NTSC Composite interface.

Figure 4-35 shows IRGB interface.

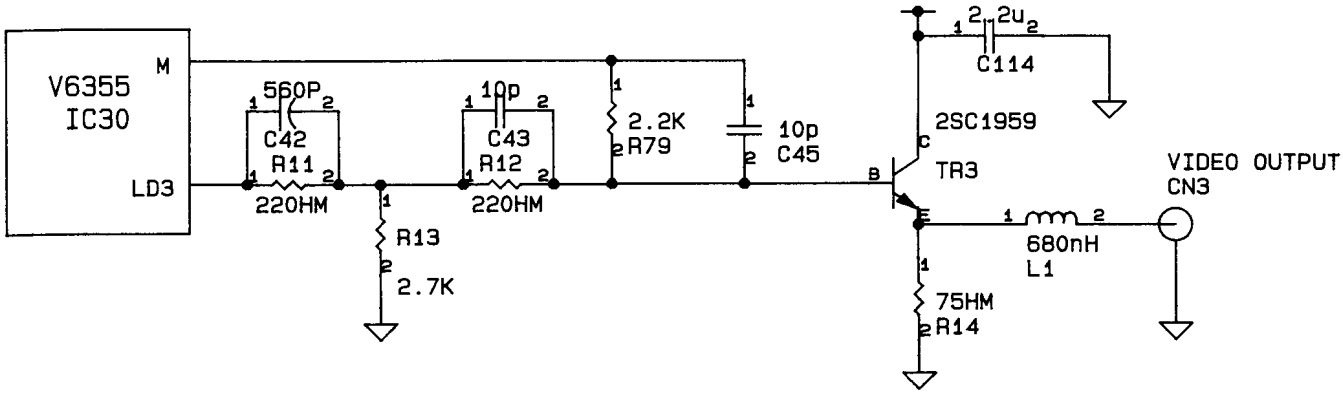


Figure 4-34. NTSC Composite Interface

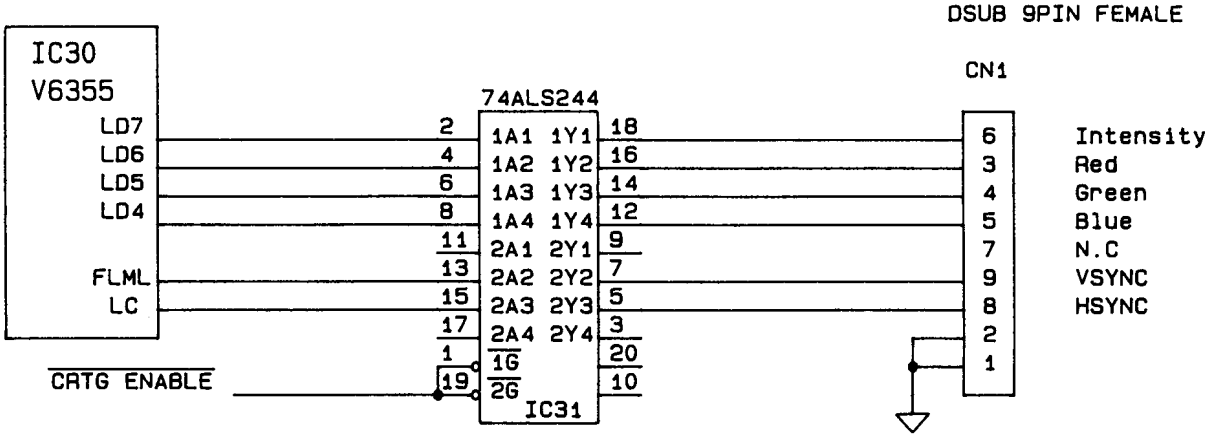


Figure 4-35. IRGB Interface

Figure 4-36 shows NTSC Composite interface timing diagram.

(Terminating resistor for Y and CH = 5.6 kOhms)

Parameter	Symbol	Min.	Typical	Max.	Unit
HSY Pulse Width	t_{HW}		4.5		μs
HSY - Color Burst Delay Time	t_{HCD}	0.8		1.3	μs
Color Burst Width	t_{CBW}		2.7		μs
Color Burst - Left Border Delay Time	t_{CLD}	0.6		1.2	μs
Left Border Width	t_{LW}	3.9		8.4	μs
Right Border Width	t_{RW}	3.9		8.4	μs
Right Border - HSY Delay Time	t_{RHD}	1.7		2.8	μs
Horizontal Display Timing Width	t_{HDW}	35.7		44.7	μs
VSY - Top Border Delay Time	t_{VTP}		764		μs
Top Border Width	t_{TW}	1.4		1.7	ms
Bottom Border Width	t_{BW}	1.3		1.8	ms
Bottom Border - VSY Delay Time	t_{BVD}		64		μs
Vertical Display Timing Width	t_{VDW}	12.2		13.0	ms
HSY Interval	t_{PH}		63.695		μs
VSY Interval	t_{PV}		16.688		ms
VSY Pulse Width	t_{VYW}		196		μs
Blanking Level	V_{BL}	1.2	1.5	1.9	V
(Black Level) - (Blanking Level)	V_B	70	85	100	mV
(SYNC Level) - (Blanking Level)	V_S	-0.35	-0.38	-0.42	V
(White Level) - (Black Level)	V_W	0.99	1.05	1.12	V
CH Offset Level	V_C	1.65	1.95	2.35	V
Burst + Side Level	V_+	0.26	0.29	0.33	V
Burst - Side Level	V_-	-0.26	-0.29	-0.33	V
CH + Side Maximum	C+	0.65	0.7	0.76	V
CH - Side Maximum	C-	-0.67	-0.72	-0.78	V

NOTE: The White level is when the RGB = 777, and the maximum amplitude of CH is when RGB = 770.

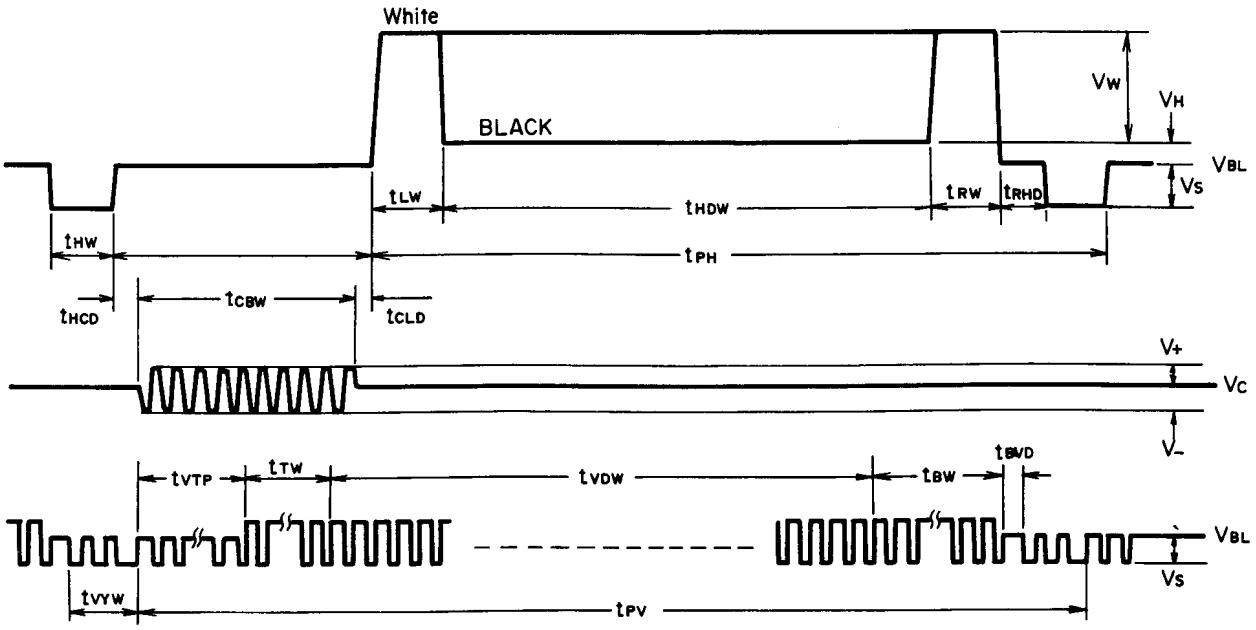
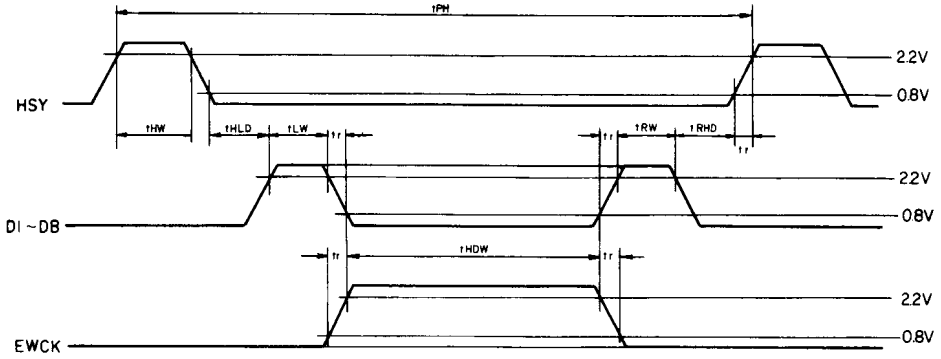


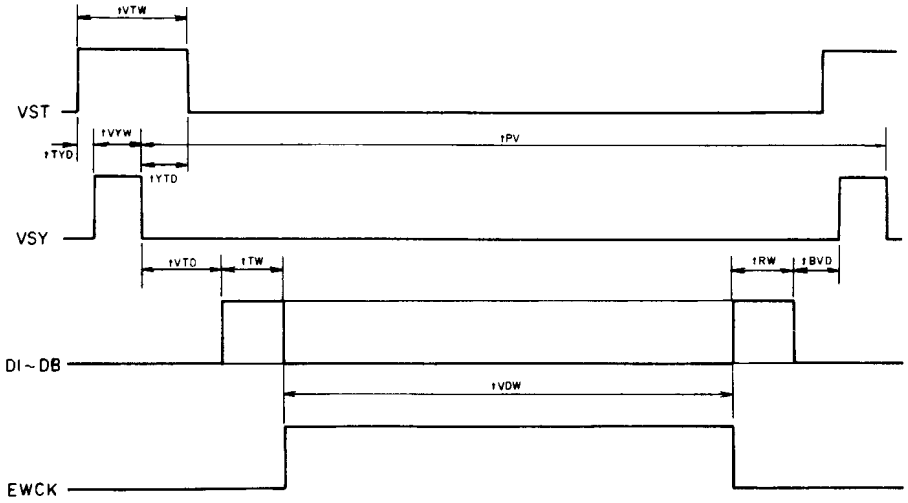
Figure 4-36. NTSC Composite Interface Timing Diagram

Figure 4-37 shows IRGB interface timing diagram.

Parameter	Symbol	Minimum	Typical	Maximum.	Unit
HSY High-Level Pulse Width	tHW		4.5		μs
HSY - Left Border Delay Time	tHLD	4.1		5.2	μs
Left Border Width	tLW	3.9		8.4	μs
Right Border Width	tRW	3.9		8.4	μs
Right Border - HSY Delay Time	tRHD	1.5		2.5	μs
Horizontal Display Timing Width	tHDW	35.7		44.7	μs
HSY Interval	tPH		63.695		μs
VSY Interval	tPV		16.688		ms
VSY - Top Border Delay Time	tVTD		764		μs
Top Border Width	tTW	1.4		1.7	ms
Bottom Border Width	tBW	1.3		1.8	ms
Bottom Border - VSY Delay Time	tBVD		64		μs
Vertical Display Timing Width	tVDW	12.2		13.0	ms
VSY High-Level Pulse Width	tVYW		196		μs
VST High-Level Pulse Width	tVTW		1019		μs
VST - VSY Delay Time	tTYD		56		μs
VSY - VST Delay Time	tTYD		764		μs
Video Output Rise, Fall Times	tr, tf			50	ns



NOTE: The timings for the R, G, and B outputs for a Linear RGB Monitor are the same as for DI to DB. The outputs, however, (offset voltage and amplitude) differ from DI and DB.
The Border width and Display Enable Timing width depend on the number of dots displayed.
For a PAL format, the VSP cycles are 20.0 ms, the Top Border time is increased by 1.7 ms, and the Bottom Border is increased by 1.5 ms.



NOTE: DI to DB and EWCK is at the low level when near HSY.

Figure 4-37.IRGB Interface Timing Diagram

IV-17. Serial Interface

The TANDY 1400LT is equipped with two serial interfaces.
RS232C interface or MODEM connector interface is changed by software.
Figure 4-38 shows a block diagram of these interfaces.

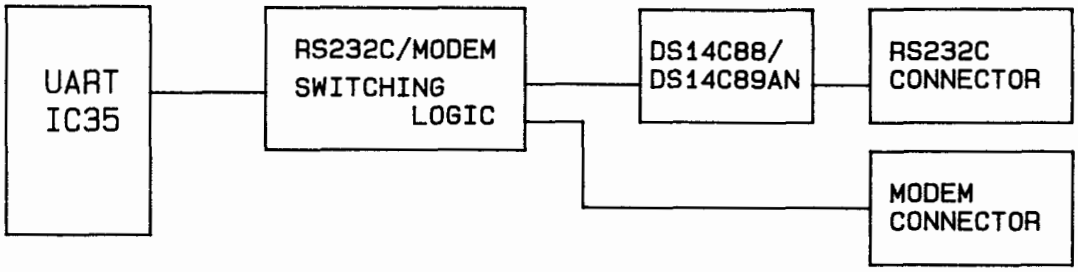


Figure 4-38. Serial Interface Block Diagram

UART

Serial data for the TANDY 1400LT is controlled by UART(TC8570P).
The UART (IC35) performs serial-to-parallel conversion on data characters received from RS232C connector or Internal Modem connector, and parallel-to-serial conversion on data characters received from the CPU.
The CPU can read the complete status of the UART (IC35) at any time during the functional operation.
Status information reported includes the type and condition of the transfer operations being performed by the UART, as well as any error conditions (parity, overrun, framing, or break interrupt).
Figure 4-39 shows the pin layout definitions of UART.

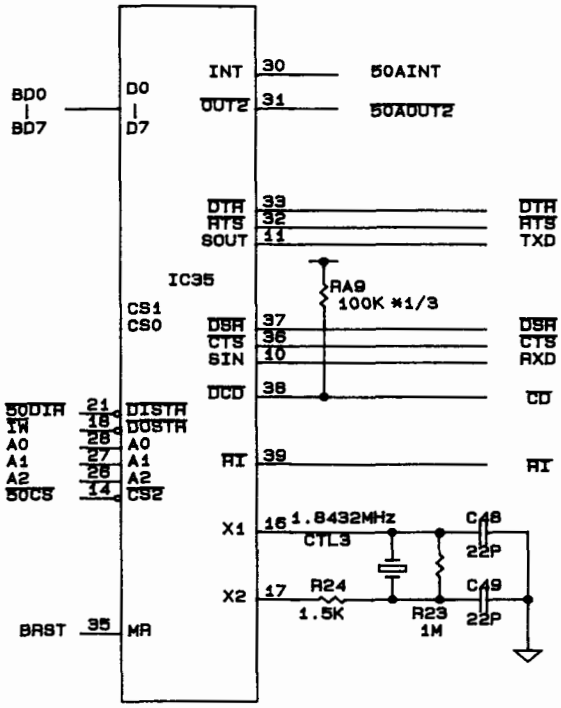


Figure 4-39. Pin Layout Definitions of UART

The UART (IC35) contains a programmable Baud Rate Generator.
The output frequency of the Baud Rate Generator is 16x the baud rate [divisor # = (frequency input)/(baud rate × 16)]. Two 8 bit latches store the divisor in a 16 bit binary format. These Divisior latches must be loaded during initialization in order to ensure desired operation of the Baud Rate Generator.
Table 4-10 shows the use of the Baud Rate Generator with crystal frequency of 1.8432 MHz .

Desired Baud Rate	Divisor Used to Generate 16 × Clock	Percent En or Difference Between Desired and Actual
50	2304	——
75	1536	——
110	1047	0.026
134.5	857	0.058
150	768	——
300	384	——
600	192	——
1200	96	——
1800	64	——
2000	58	0.69
2400	48	——
3600	32	——
4800	24	——
7200	16	——
9600	12	——

Table 4-10. Baud Rate Generator (1.8432 MHz)

TO RS232C CONNECTOR / TO MODEM CONNECTOR SWITCHING CIRCUIT
The switching circuit is generated in the GATE3. MOD/$\overline{RS}$ signal is selectable by the software. Figure 4-40 shows the block diagram of GATE3 (Switching logic)

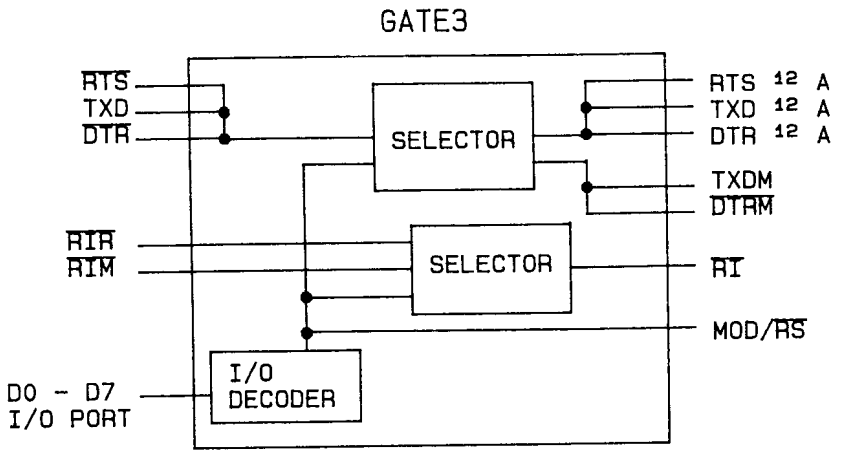


Figure 4-40. Switching Logic (RS232C, MODEM)

RS232C Interface Circuit

The TANDY 1400LT use DS14C88/DS14C89AN for Line Driver/Receiver.

The DS14C88/DS14C89AN translates standard TTL or CMOS logic levels to/from levels conforming to RS232C.

Figure 4-41 shows RS232C interface circuit.

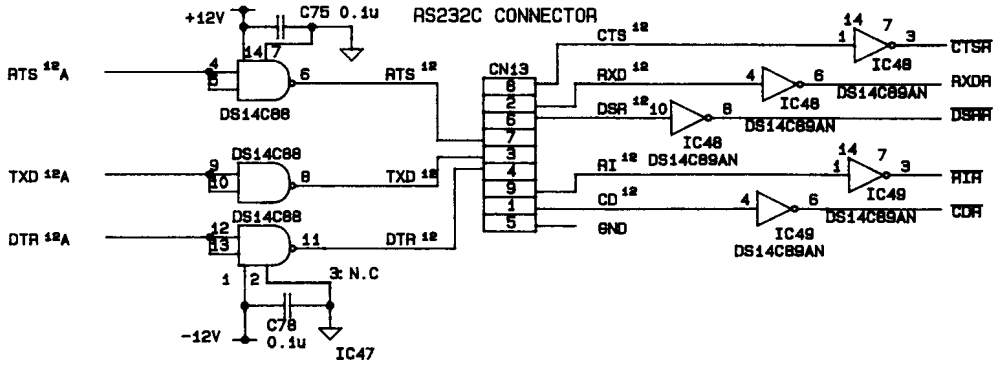


Figure 4-41. RS232C Interface Circuit

Figure 4-42 shows internal modem connector and peripheral circuitry.

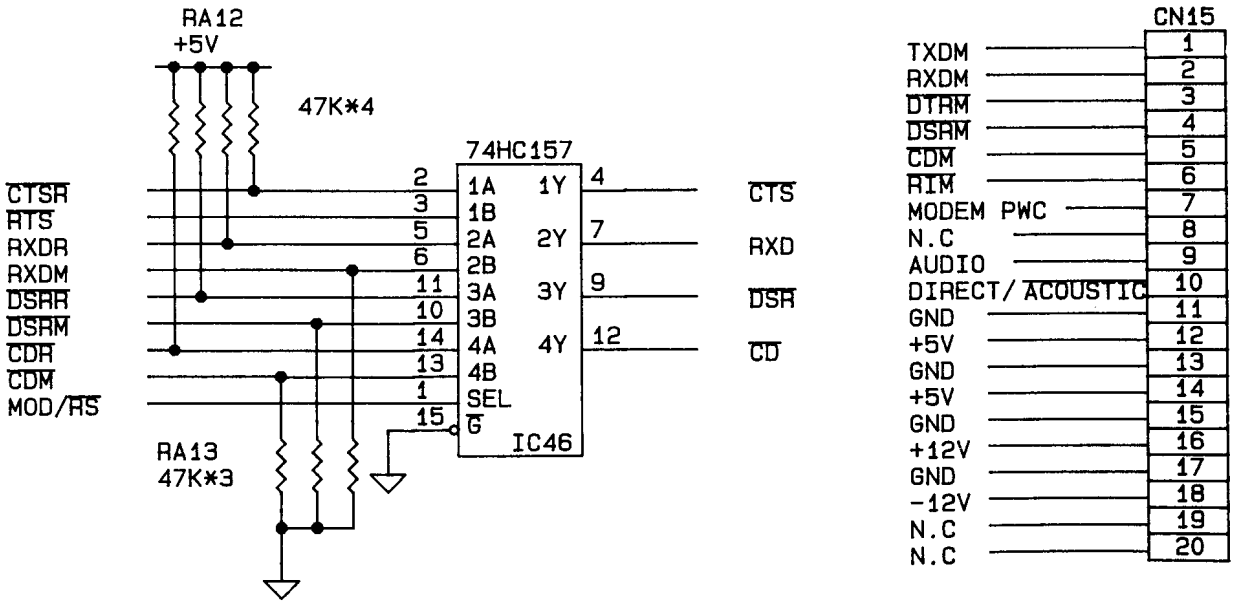


Figure 4-42. Internal MODEM Connector and Peripheral Circuitry

IV-18. RTC

The RTC: RP5C15 (Real Time Clock) has an internal counter for time (hours, min, sec.) and date (100 years, leap years, months, dates, and days-of-the-week). Time can be written to or read from the RTC in the same way as writing to or reading from the RAM. Time counting function is maintained by the back up battery (BATT 1 even when the system is turned off. The RTC has an alarm function but the TANDY 1400LT does not use it.)
Figure 4-43 shows RTC and peripheral circuitry.
The following external parts are required for constructing the oscillator circuit.

1. A quartz oscillator with frequency of 32.768kHz
2. Two capacitors (including one trimmer capacitor)

The accuracy of the oscillation frequency should be measured by using a standard clock signal to be output from terminal 3 (CKOUT). The accuracy of the oscillation frequency can be checked by connecting the CKOUT terminal to frequency counter. (The measuring probes of a frequency counter or oscilloscope should not be connected directly to the OSCIN (Pin 16) or OSCOUT (Pin 17) terminal, since the capacity of the probes will alter the oscillation conditions and make correct measurement impossible.)

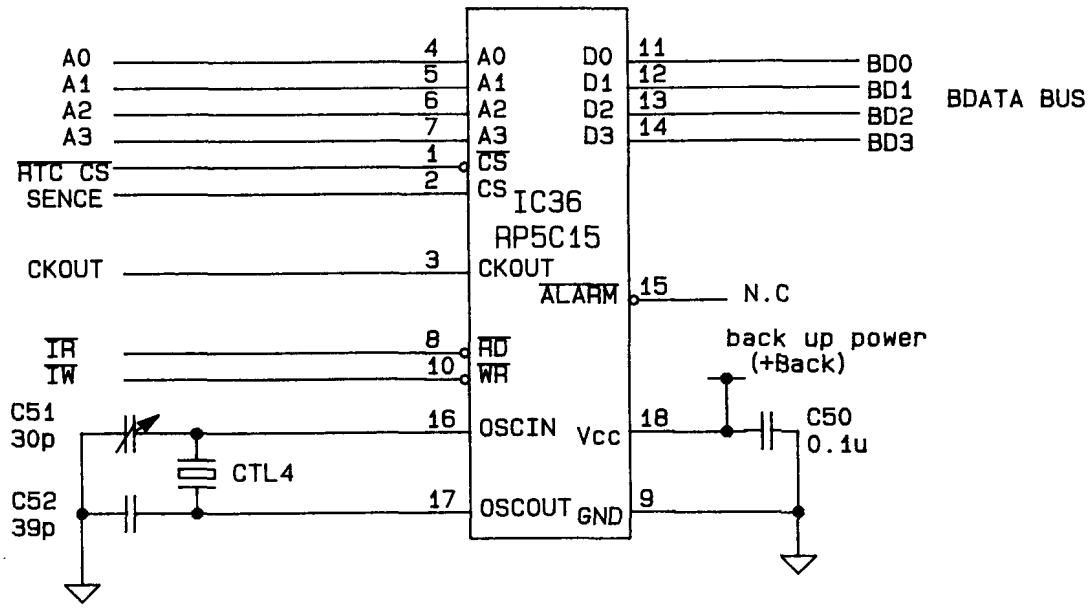


Figure 4-43. RTC and peripheral circuitry

IV-19. Speaker Circuit

The system unit has a 28mm (1.1inch) audio speaker. The speaker control circuits and driver are on the MAIN PCB. The speaker driver is capable of about 0.2 watts of power. The control circuits allow the speaker to be driven three different methods.

1. Direct program control with an I/O address, 61H bit 1, may be toggled to generate a tone pulse.
2. Output from Channel 2 of the timer counter, may be programmed to generate a tone pulse.
3. PRCLK clock input to timer counter can be modulated with an I/O address, 61H bit 0.

Volume Control

The speaker output level is controlled by the variable resister that is located in the battery compartmet. By turning it clockwise, you can increase the speaker output, and by turning it counter clockwise, you can decrease the speaker output.

Figure 4-44 shows the Speaker block diagram.

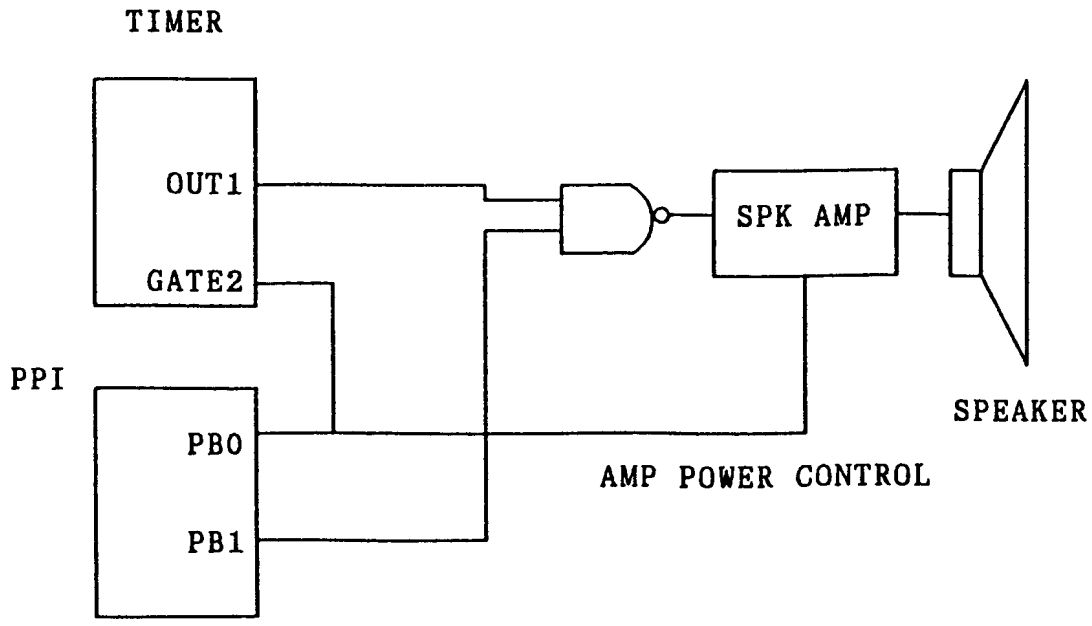


Figure 4-44. Speaker Block Diagram

IV-20. Power Supply

The system DC power supply has an approximately 13 watt, 4 Voltage-level regulator. It is integrated into the system unit and supplies power for the system unit, External keyboard, and its option.
The supply provides 2.5A of +5VDC + 1% or -5%, 60mA of +12VDC ± 5%, 60mA of -12VDC ± 10% and 20mA of -15VDC ± 10%.
The system unit takes approximately (0.3) to (1.8)A of +5VDC, thus allowing approximately (0.7) A of +5VDC for the adapters in the Exbus slot and modem slot. The +12VDC and -12VDC are used for powering the Electronic Industries Association (EIA) drivers for the communications and analog circuits, in the main PCB. The -15VDC level is used for LCD bias.

Output control

Control 1 : +5V	- High ON
Control 2 : +12V, -12V, +15V	- Low ON

Input Requirements
The normal power requirements are listed below.
Input Voltage

Normal input	15V DC
Minimum input	13.5V DC
Maximum input	20V DC

Input requirement

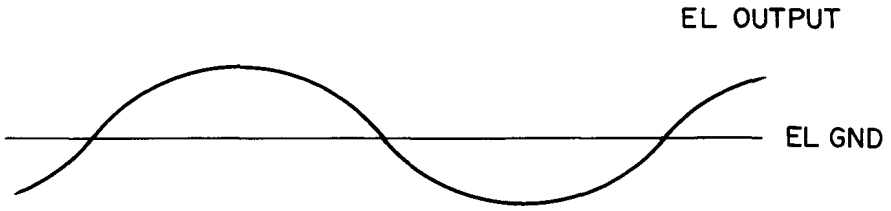
Current	700mA at 15V DC

Outputs

Voltage	Max. power (Amp.)	Regulation
+5V	2.5 A	+1% or -5%
+12V	0.06 A	+5% or -5%
-12V	0.06 A	+10% or -10%
-15V	0.02 A	+10% or -10%

EL Invertor
1. Output voltage frequency
   Input Voltage - 12V = 116V, Vrms = 328Vp-p : 580-700Hz
   - 15V = 140V, Vrms = 396Vp-p : 580-700Hz

2. Output waveform



Output level and frequency vary from unit to unit.

Figure 4-45. EL Output Waveform

Power Source

Main Battery 12V, 2200mAh, Nickel-Cadmium battery.

Back up Battery A Nickel-Cadmium battery of 3.6V 50mA is used to hold the Time Data of RTC.

Battery Voltage Warning

The first warning is indicated by Low Battery RED LED and 2 beeps. The user is instructed to charge the battery voltage to 11.7V ~ 11.9V. After the first warning, the system can be used for about 30 minutes with the FDD 10% duty.

The second warning is indicated by Low Battery RED LED flashing and 5 beeps times. The user is instructed to shut down the system at a battery voltage of 10.8 ~ 11.4V. User should close current task file. If used after Low Battery warning, the system shuts down and loses all RAM data.

Power Save Mode

When nothing is input for about 1 ~ 239 minutes (software selectable) after the last keying in, the system automatically turns to standby mode. Pressing any key will bring the computer out of STAND-BY MODE. The program being used when STAND-BY MODE is engaged is maintained intact.

1. The time of auto standby mode can be set from 1 minute to 3 hours 59 minutes in set up mode.
2. In standby mode, a GREEN LED lights.
3. In standby mode, memory contents will be maintained by main battery over 11 hours, at the condition of full charge. When main battery is discharged, memory contents are lost. RED LED of Low Battery warning is displayed in standby mode too.
4. Input Power rating (AC adapter) voltage 8 ~ 20V (15V, 700mA center ground).
5. Current consumption (TYPICAL DATA)

	CRT	LCD
Normal use mode	240mA	470mA
FDD SEEK	430mA	700mA
FDD MOTOR ON	350mA	570mA
STANDBY MODE	160mA	

5V Output Voltage Circuit

The Power Supply circuit of 5V output consists of a step-down switching regulator. As shown in Figure 4-46, the circuit has no transformer; the input and output terminals are direct currentwise common. Therefore it is free from the trouble caused by a linkage-inductance and provides a miniaturized and effective Power Supply.

In the circuit, an input voltage VI is turned ON/OFF by a switching transistor (Tr) and is converted into a square wave, which is smoothed through an LC filter. This method is used where an output voltage is lower than an input voltage. This Power Supply circuit operates at an input voltage as low as 8V.

The operations of the blocks of 5V Power Supply circuit are as follows.

Block ① μPC494, a controller of switching regulator, controls the ON/OFF of a switching transistor TR511 ② (Figure 4-48).

Block ② TR511 is the switching transistor shown as Tr in Figure 4-46.

Block ③ An LC filter which smooths the square wave resulted from TR511 switching.

Block ④ In case TR511 is locked ON for some reason, SCR500 turns on and prevents the input voltage VI (Figure 4-46) from directly appearing at the output guiding it to the ground. Thus it protects the connected systems form failure.

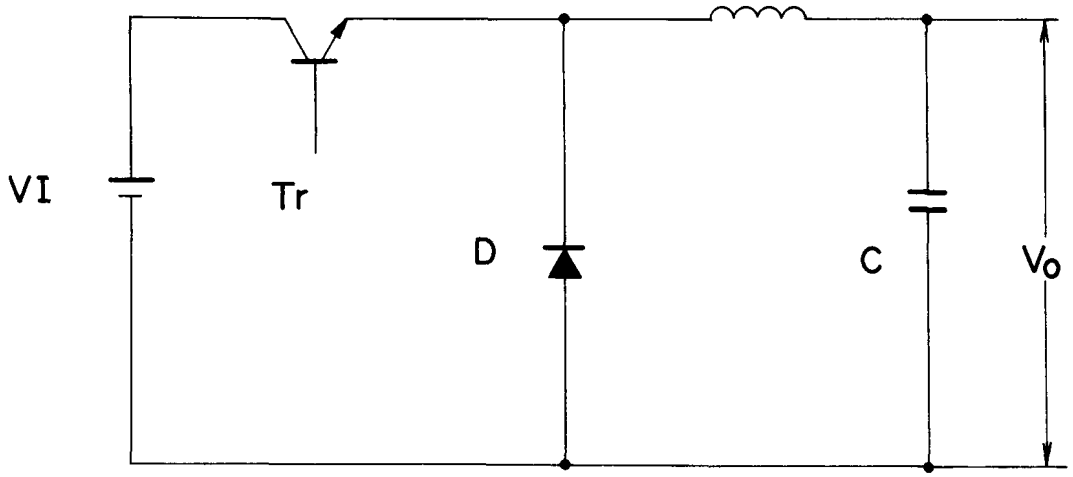
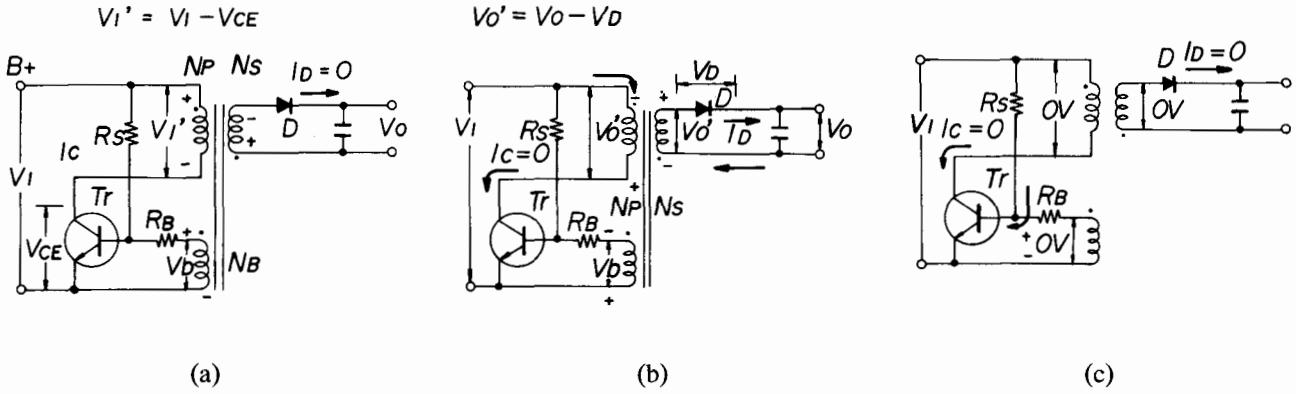


Figure 4-46. 5V equivalent circuit

12V Output Voltage Circuit

This is a one transistor self-excited DC/DC converter, which is called R.C.C. (Ringing Choke Converter). Figure 4-47 shows the principle of the circuit.



(a) (b) (c)

Figure 4-47. R.C.C (Ringing Choke Converter)

(a) When the power is supplied to VI (B+), Tr turns on, and Ic flows through the primary winding of the transformer.
By this current, voltage (Vb) is induced to the base winding, then Tr immediately reaches saturation.

(b) Tr can no longer maintain saturation. Therefore, Tr turns off immediately, then the voltage Vo is created by the magnetic energy stored in the transformer, and the voltage is sent to the output Vo through the diode D.

(c) When the energy stored in the transformer is discharged, the output current ID diminishes and reaches zero. However, Tr turns on immediately by the base voltage Vb which is induced from the primary winding, and the above procedures are repeated.

The operation of the blocks of 12V Power Supply circuit is as follows:

Block ⑤ The Block operates lick a Boot-up register Rs in Figure 4-47. The Block is made up of Boot-up circuit, output voltage controller and shut-down circuit, and the block controls TR508 ⑥.

Block ⑥ This switching transistor operates like a transistor in Figure 4-47.

Block ⑦ This transformer creates +12V, −12V and −15V output voltages.

EL Drive Circuit

Figure 4-49 shows the self-excited DC/AC inverter circuit.

The circuit converts DC to AC by switching at TR512 ⑧, and feeds it to the primary winding at T501 ⑨. The voltage and the frequency at the secondary winding at T501 ⑨ depend on the inductance and load capacitors. Characteristic changes of EL by aging affect the voltage and frequency at the secondary winding.

Others

Block ⑩ This noise-filter absorbs line-noise from AC-adapter.

Block ⑪ This is the resistor for the toricle charge to the Main Battery.

Block ⑫ When the unit is used with AC-adapter, this stabilized circuit prevent EL-flashing by change of +V in SEEK mode of FDD, in Figure 4-50.

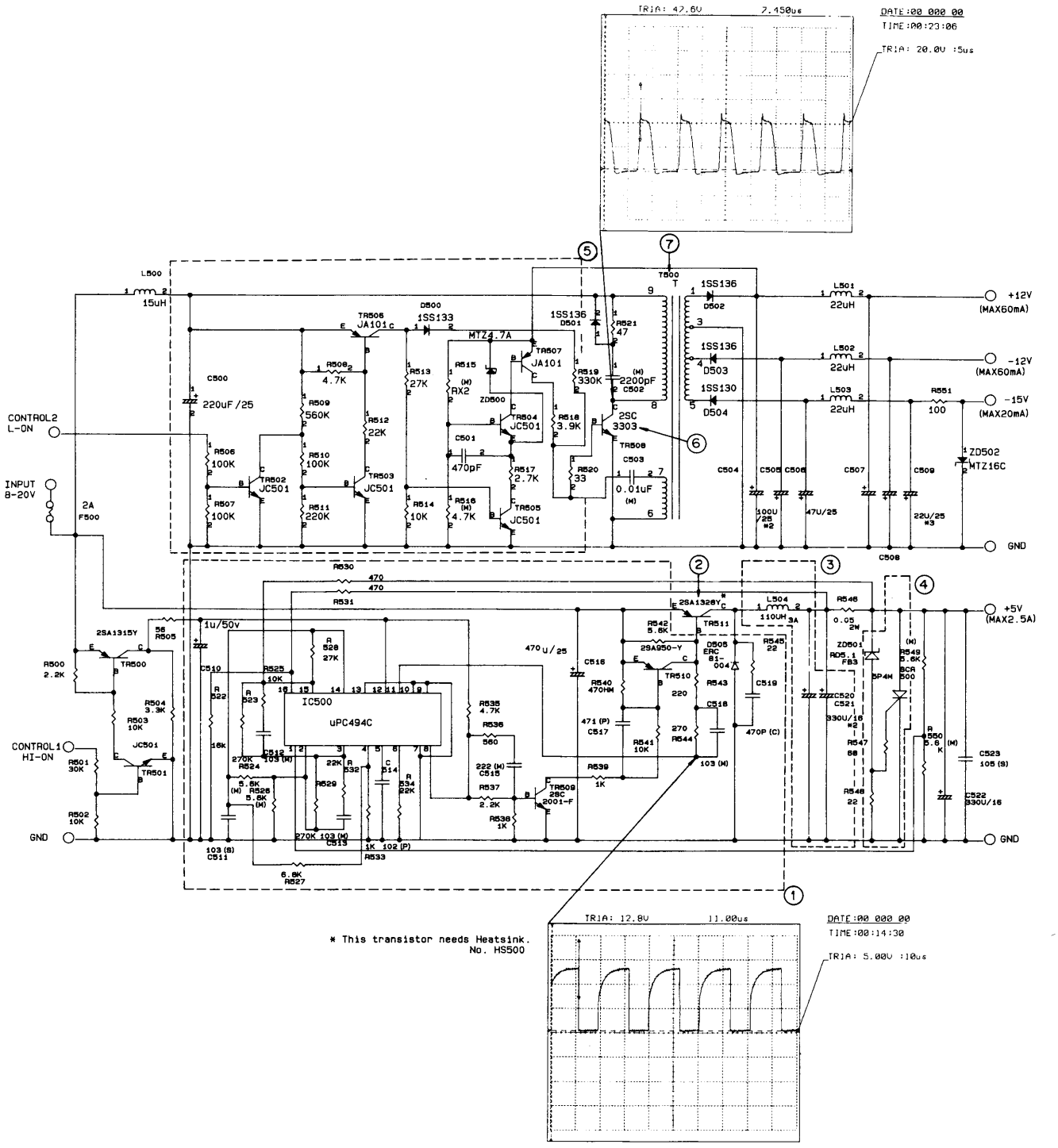
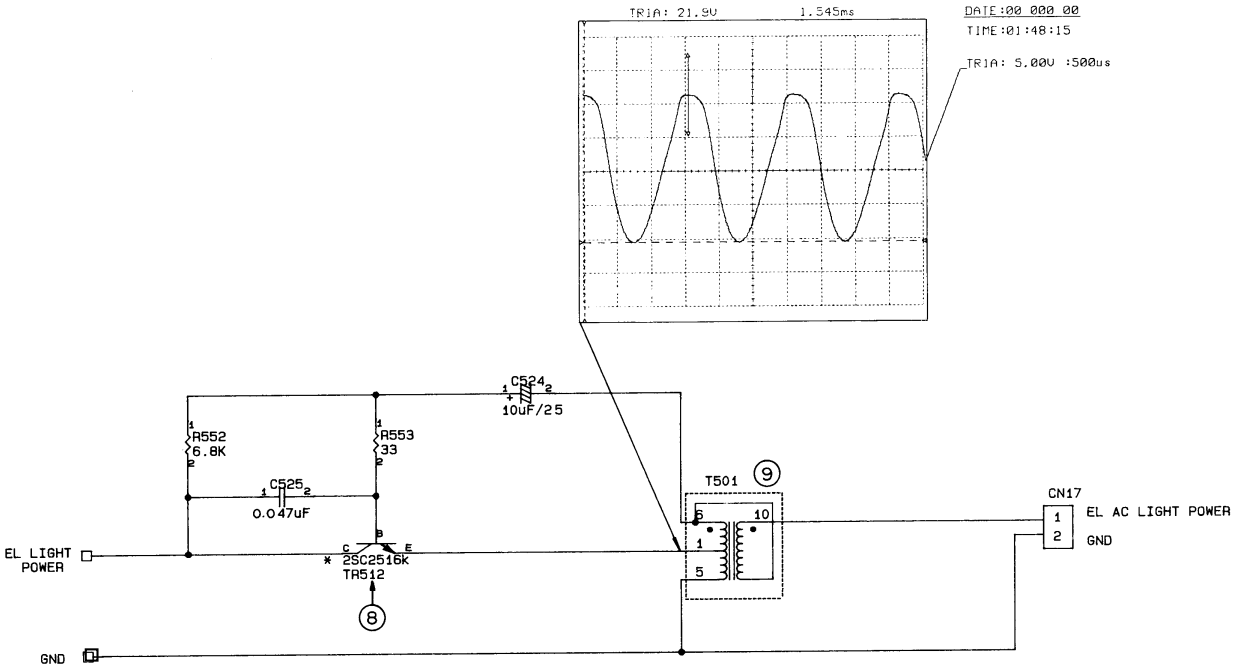


Figure 4-48. Power PCB Circuit Diagram-1



* This transistor needs Heatsink.
No. HS501

Figure 4-49. Power PCB Circuit Diagram-2

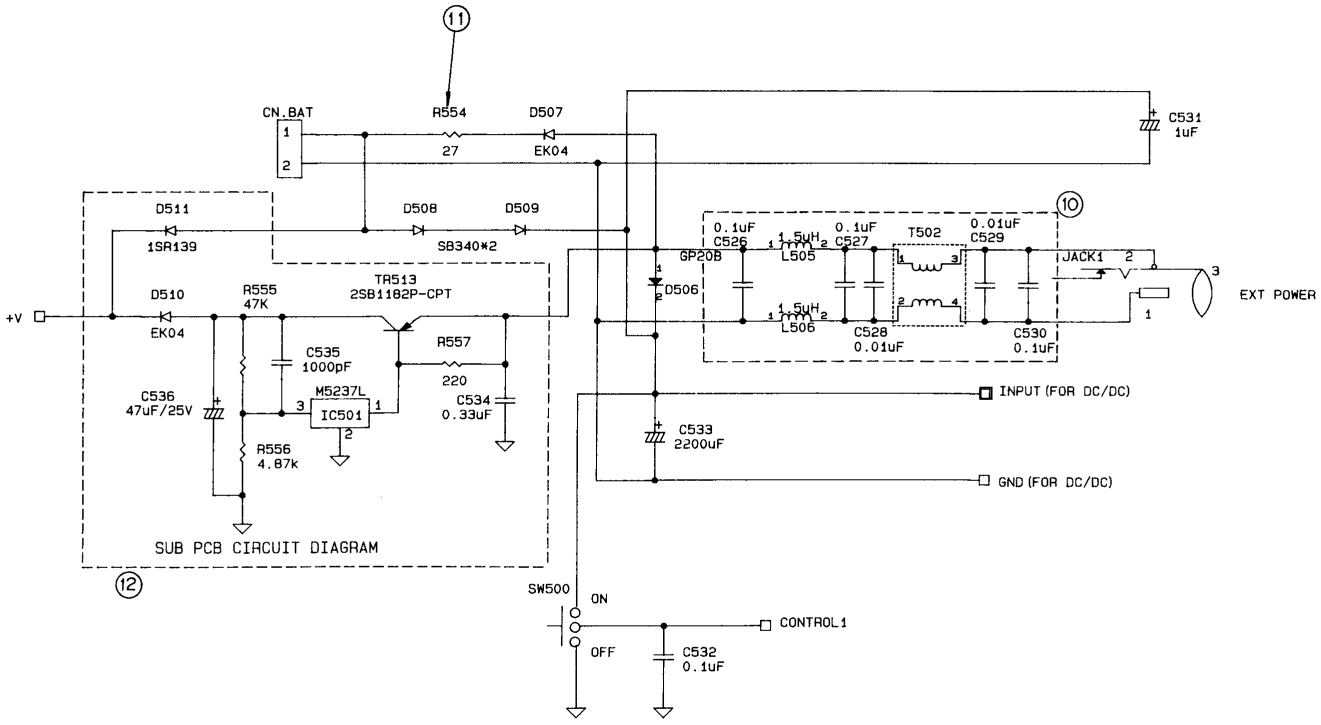


Figure 4-50. POWER PCB Circuit Diagram-3

IV-21. Option

EXPANSION BUS (Option Interface card)

The interface card is a small card installed into the expansion bus connector accessed at the rear of the TANDY 1400LT.

This card relays signals transferred between the TANDY 1400LT system board and optional expansion box.

Table 4-11 shows the EXPANSION I/O Connector pin assignment.

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	N.C	31	A19
2	+5V	32	D0
3	*ENABLE	33	D1
4	N.C	34	D2
5	N.C	35	D3
6	*DACK0	36	GND
7	IRQ3	37	D4
8	N.C	38	D5
9	GND	39	D6
10	A0	40	D7
11	A1	41	*EMW
12	A2	42	*EMR
13	A3	43	GND
14	A4	44	*EIW
15	A5	45	*EIR
16	A6	46	*TC
17	A7	47	ALE
18	GND	48	*BRST
19	A8	49	*DACK1
20	A9	50	IRQ2
21	A10	51	GND
22	A11	52	+5V
23	A12	53	ECLK
24	A13	54	IRQ5
25	A14	55	DR3
26	A15	56	*DACK3
27	GND	57	BEN
28	A16	58	DR1
29	A17	59	IOREADY
30	A18	60	GND

Table 4-11. Expansion I/O Connector

The interrupt signals for expantion bus supported by Tandy 1400 LT are IRQ2, IRQ3 and IRQ5. Other interrupt signals are used in internal logic. And DMA signals for expansion bus are DACK1 and DACK3. Other DMA signals are used in internal logic.

Signal Name	I/O	Description
ECLK	O	Clock: This is the system clock. It has 2 speed modes. (4.77MHz, 7.16MHz). The clock has a 50% duty cycle
*BRST	O	RESET: This is a the system reset. This signal is synchronized to the falling edge of clock and is active LOW
A0-A19	O	Address Bits 0-19: These lines are generated by either the CPU (V20) or the DMA controller (82C37). They are active HIGH.
D0-D7	O	Data Bits 0-7: These lines are active HIGH.
ALE	O	Address Latch Enable: This is provided by the Bus Controller (μPD71088). The CPU addresses are latched with the falling edge of ALE.
IOREDY	O	I/O Channel Ready: This line is pulled low by a memory or I/O device to lengthen I/O or memory cycle.
IRQ 2,3,5	I	Interrupt Requests 2,3,5: These lines are used to signal the processor that an I/O device requires attention.
*EIR	O	I/O Read Strobe: This signal is active LOW.
*EIW	O	I/O Write Strobe: This signal is active LOW.
*EMR	O	Memory Read Strobe: This signal is active LOW.
*EMW	O	Memory Write Strobe: This signal is active LOW.
DR1 & 3	I	DMA Requests 1 and 3: These lines are asynchronous channel requests used by peripheral devices to gain DMA service. A request is generated by bringing DR1 and, 3 lines must be held high until the corresponding DACK line goes active.
*DACK0,1 &3	O	DMA Acknowledge 0, 1 & 3: These lines are used to acknowledge DMA requests and refresh system DRAM (DACK0). They are active LOW.
BEN	O	Address Enable: This line is used to degate the CPU and other devices from the I/O channel to allow DMA transfers to take place. This signal is active HIGH. When this line is HIGH, the DMA Controller (82C37) has control of the lines (address bus, data bus read and write strobe: memory and I/O)
*TC	O	Terminal Count: This line provides a pulse when the terminal count for DMA channel is reached. This signal is active LOW.
*ENABLE	O	ENABLE: This line maintains a High level when internal devices are selected (ROM. RAM, VRAM, and I/O)
+5V	→	+5V +1%, -5% Max 200m Amps available on the bus.
GND	→	Power Return for +5V

INTERNAL MODEM CONNECTION

TANDY 1400LT has a Internal MODEM CONNECTOR (20 Pin card edge type)
Table MODEM shows the internal MODEM connector pin assignments.

Pin No.	Signal Name	Pin No.	Signal Name
1	TXDM	11	GND
2	RXDM	12	+5V
3	*DTRM	13	GND
4	*DSRM	14	+5V
5	*CDM	15	GND
6	*RIM	16	+12V
7	MODEM PWC	17	GND
8	N.C	18	-12V
9	AUDIO	19	N.C
10	DIRECT/*ACOUSTIC	20	N.C

Table 4-12. MODEM

Signal Name	I/O	Description
TXDM	O	Transmitted Data: This signal is the serial data output for the communication link. This terminal is set to the marking (logic 1) state upon a RESET operation.
RXDM	I	Received Data: This signal is the serial data input from the communication link
*DTRM	O	Data Terminal Ready: When this signal is active LOW, it informs the MODEM that the UART is ready to communicate. *DTRM signal is set to HIGH upon a RESET operation. *DTRM signal is forced to its inactive HIGH during loop mode operation.
*DSRM	I	Data Set Ready: When this signal is active LOW, it indicates that the MODEM is ready to establish the communication link and transfer data with UART.
*CDM	I	Carrier Detect: When this signal is active LOW, it indicates that the data carrier has been detected by the MODEM.
*RIM	I	Ring Indicator: When this input is active LOW, it indicates that the ringing signal has been received by the MODEM.
MODEM PWC	O	MODEM Power Control: This signal is MODEM power control signal and is active HIGH.
AUDIO	I	Audio: Condensor cut signal (to AUDIO AMP.)
DIRECT/*ACOUSTIC	O	Direct/* Acoustic: Direct MODEM, acoustic MODEM select signal. 1: Direct, O: Acoustic
+5		+5V +1%, -5% Max 180 mA available on the connector.
+12V		+12V +5%, -5% Max 40mA available on the connector.
-12V		-12V +10%, -10% Max 50mA available on the connector.
GND		Power Return for +5V, +12V and -12V.

*All INPUT/OUTPUT signal are TTL level voltage (0/5V)

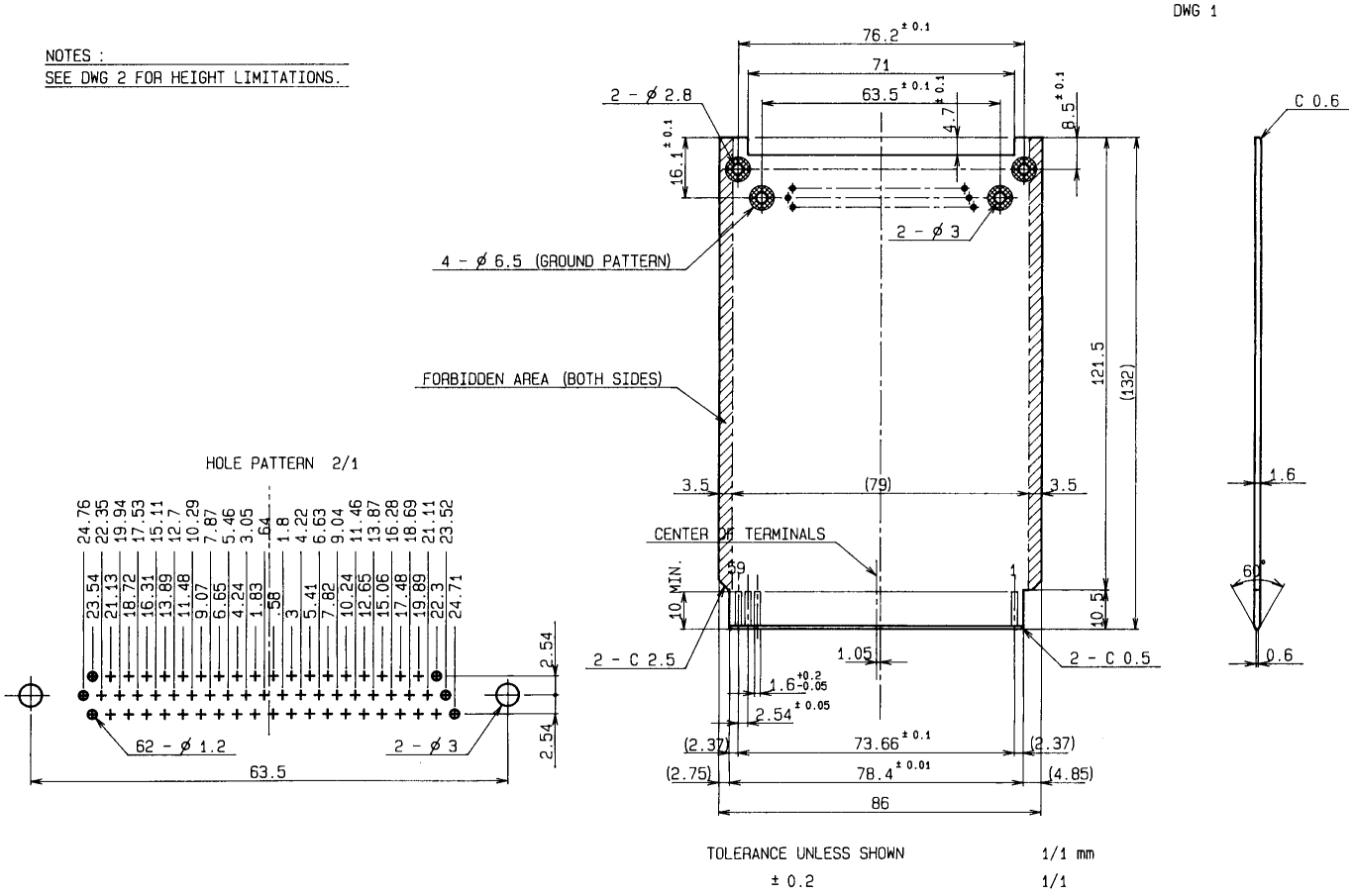
EXPANSION BUS PCB

Mechanical Drawing

DWG 1

NOTES :

SEE DWG 2 FOR HEIGHT LIMITATIONS.



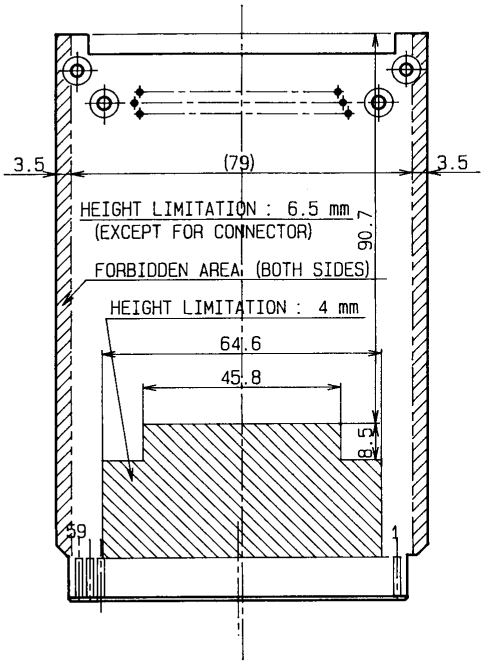
TOLERANCE UNLESS SHOWN ± 0.2

1/1 mm

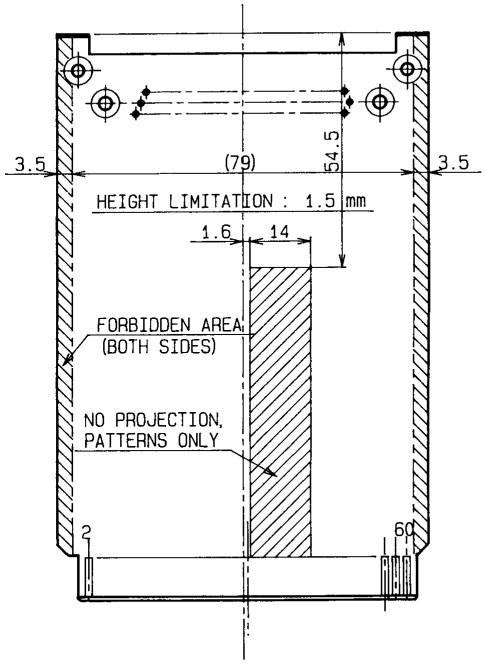
1/1

DWG 2

PARTS SIDE



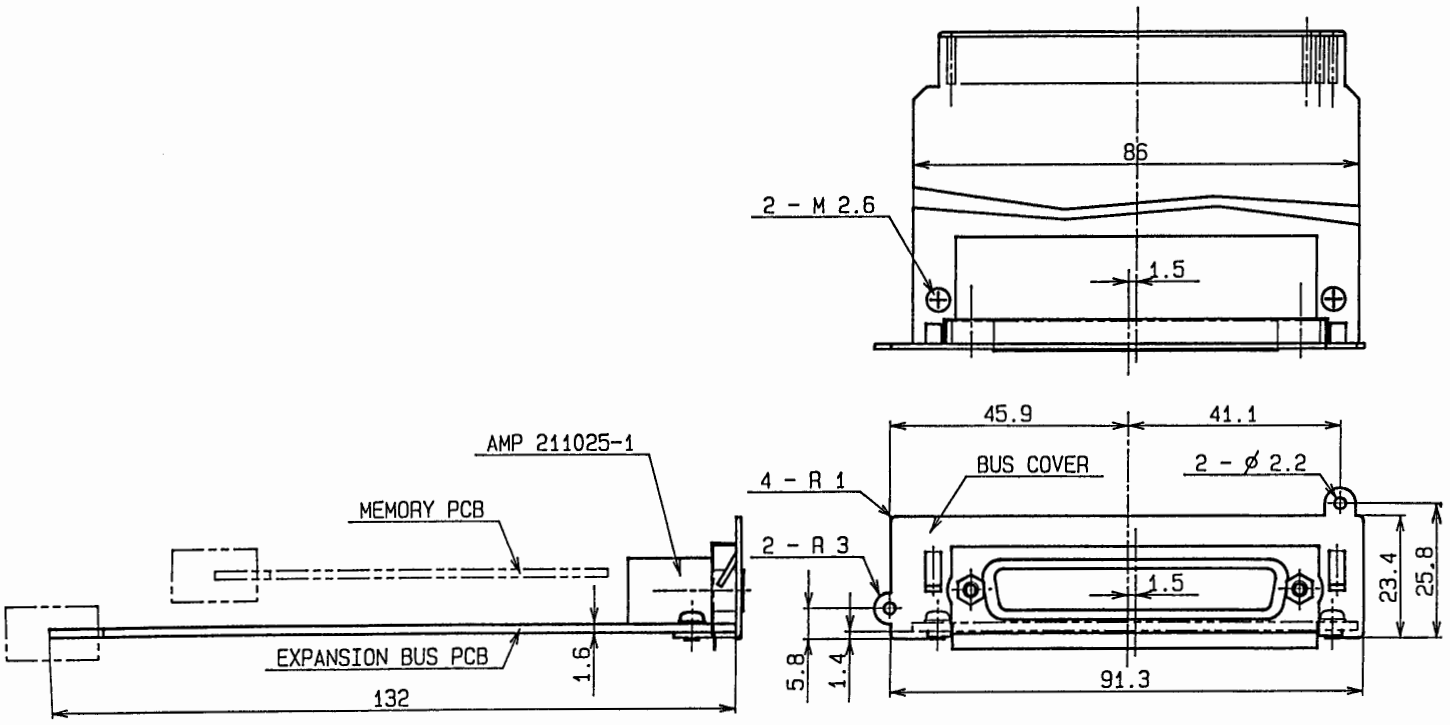
SOLDER SIDE



1/1 mm

1/1

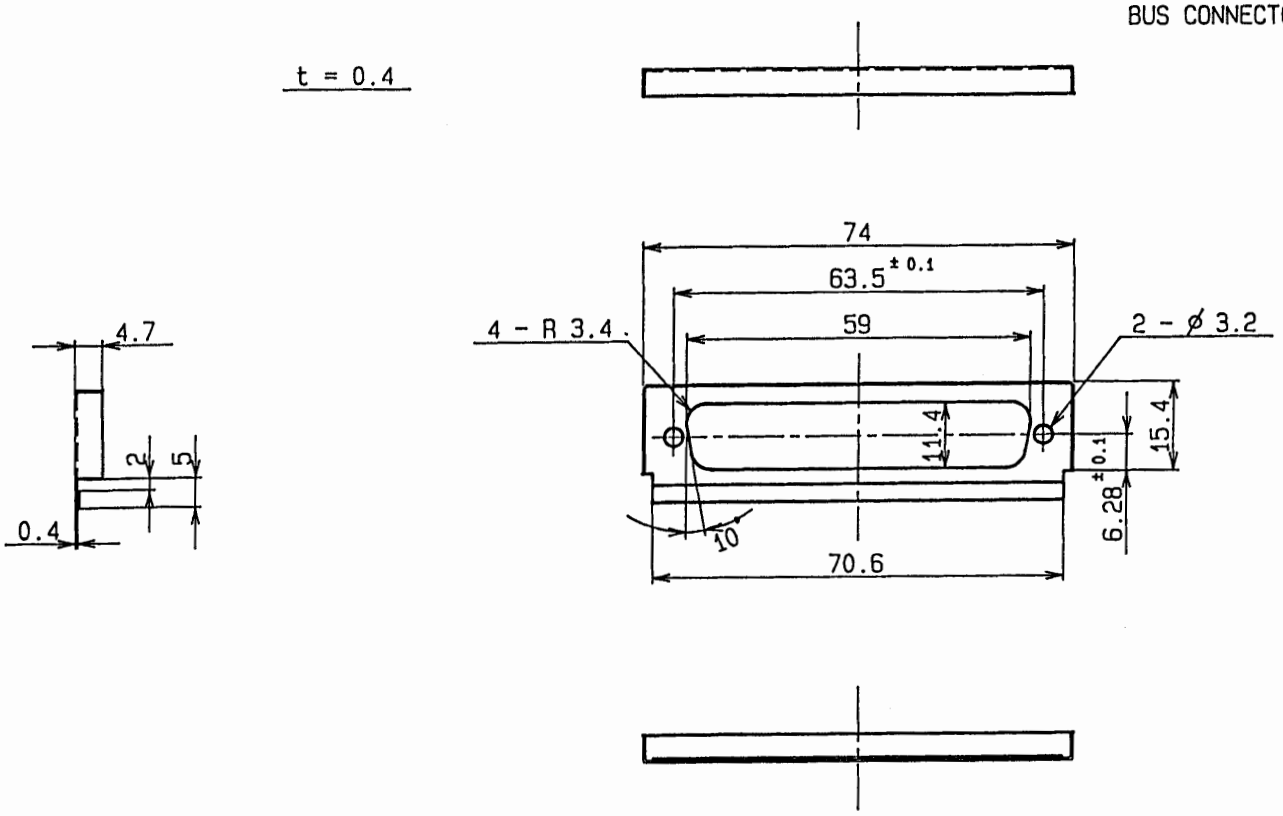
EXPANSION BUS CARD



1/1 mm
1/1

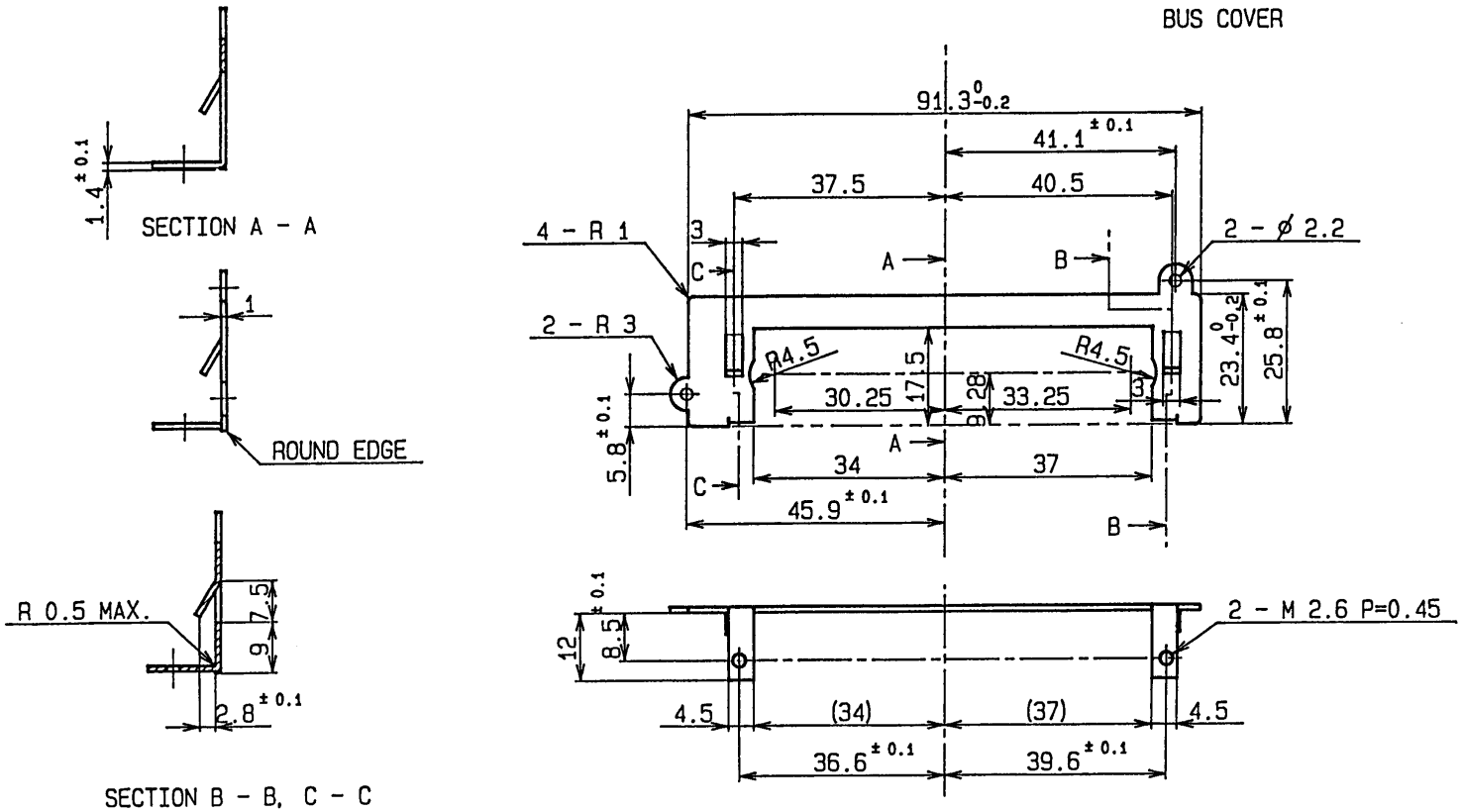
BUS CONNECTOR COVER

t = 0.4



± 0.2

STEEL, ZINC COATING
1/1 mm
1/1



± 0.2

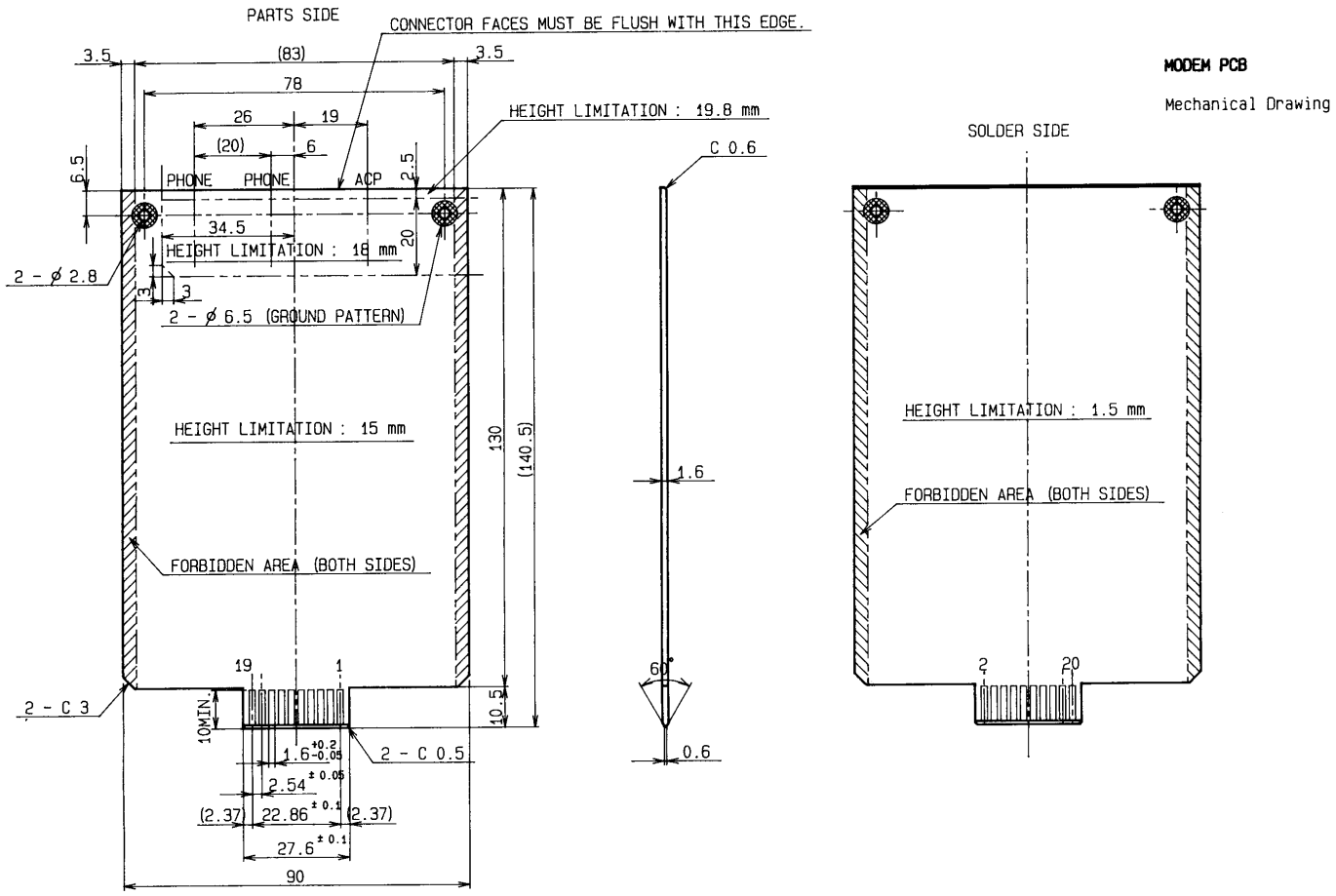
STEEL, ZINC COATING

1/1 mm

1/1

MODEM PCB

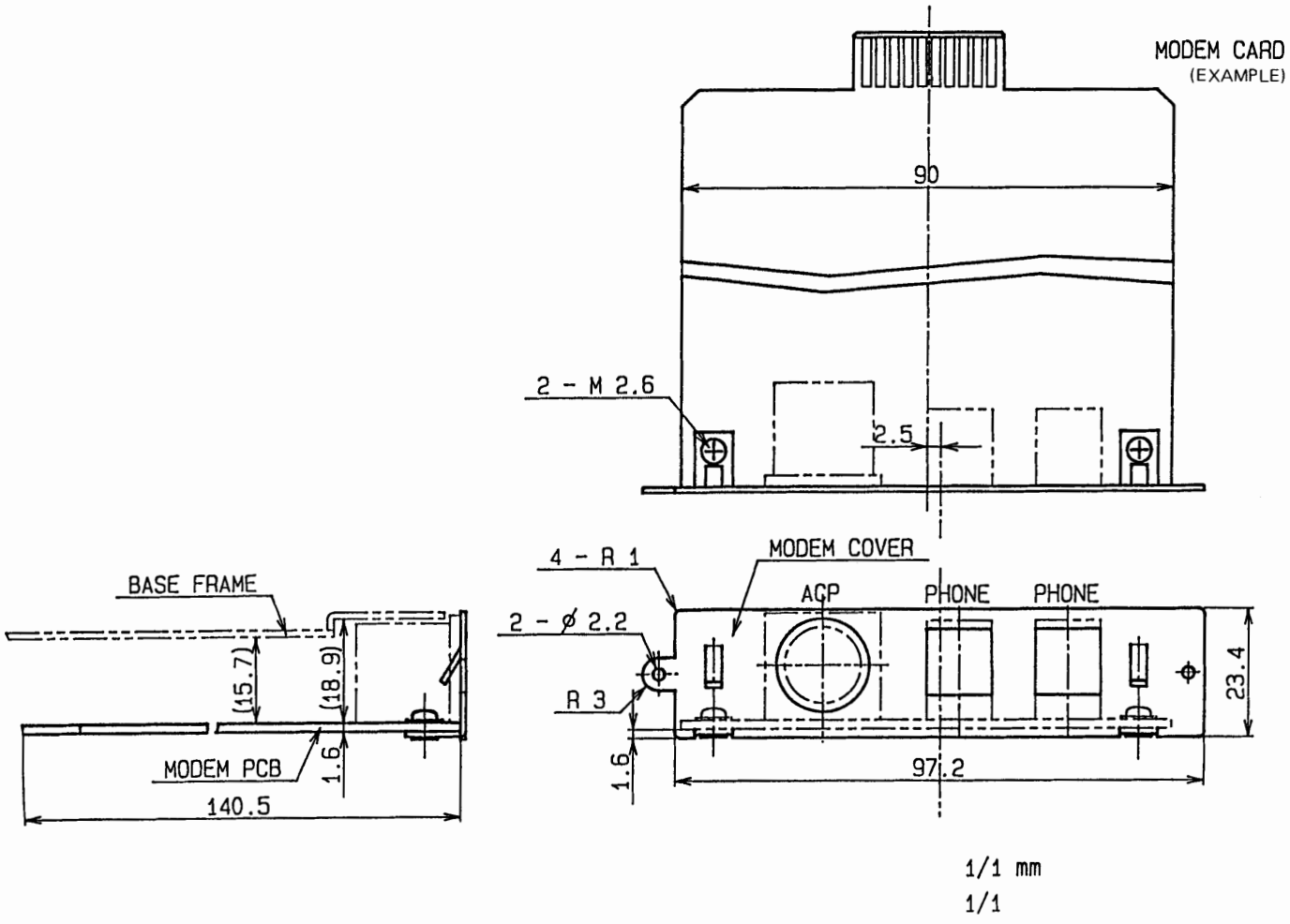
Mechanical Drawing



TOLERANCE UNLESS SHOWN ± 0.2

1/1 mm

1/1

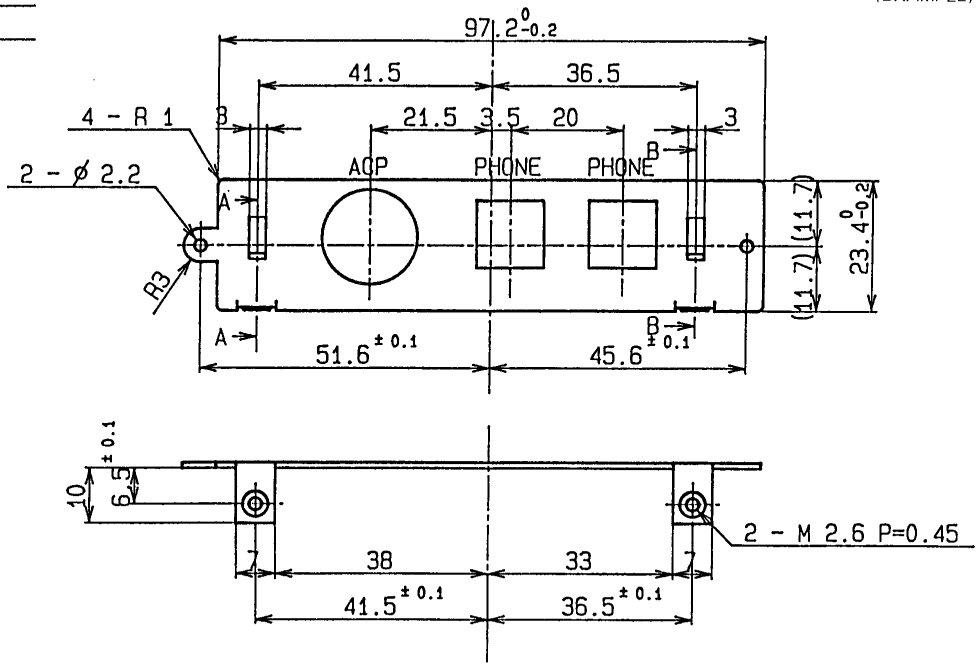


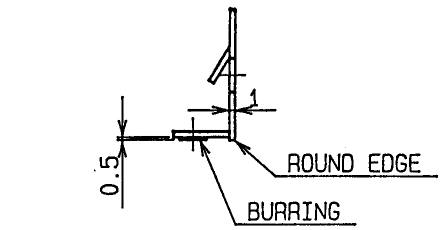
1/1 mm
1/1

NOTES :

1. THE DIMENSIONS OF THE CONNECTOR OPENINGS MAY VARY WITH PARTS.

MODEM COVER
(EXAMPLE)





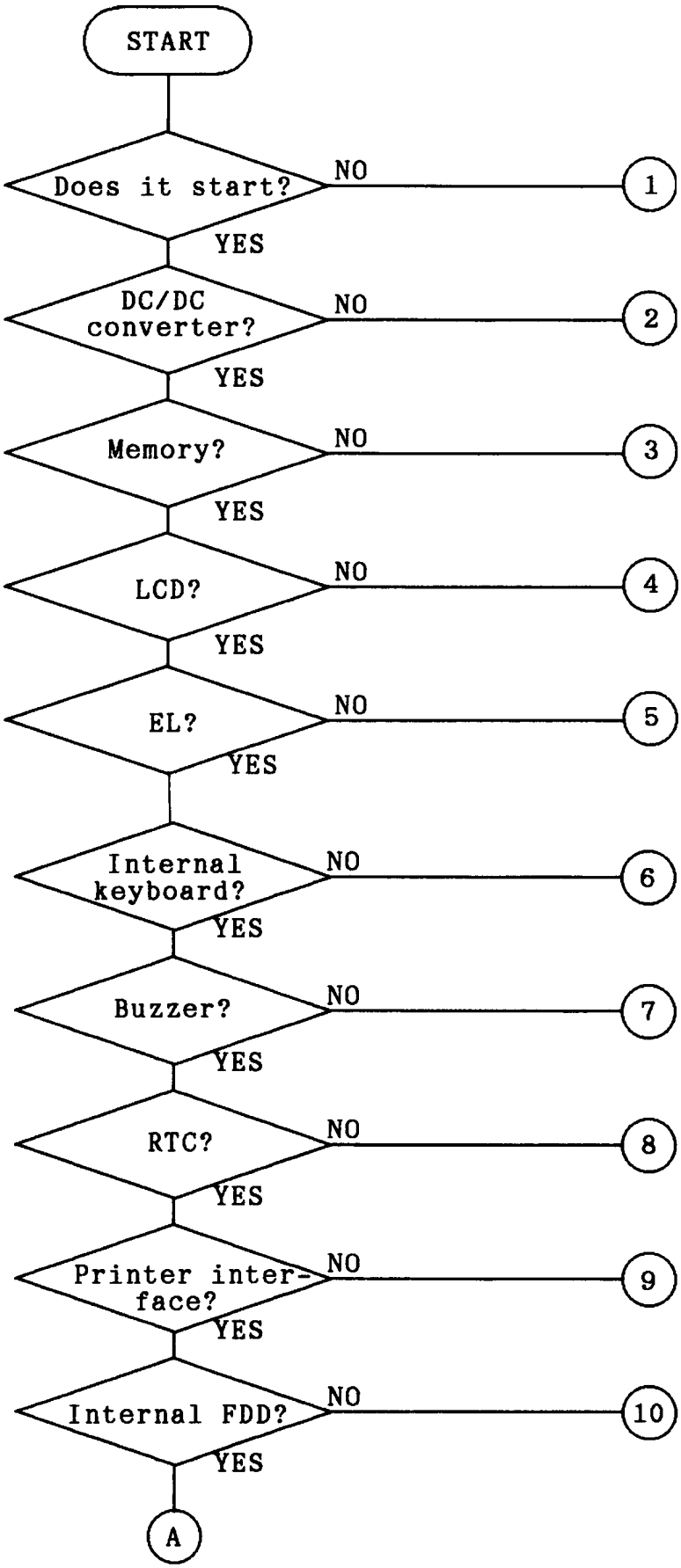
SECTION A - A, B - B

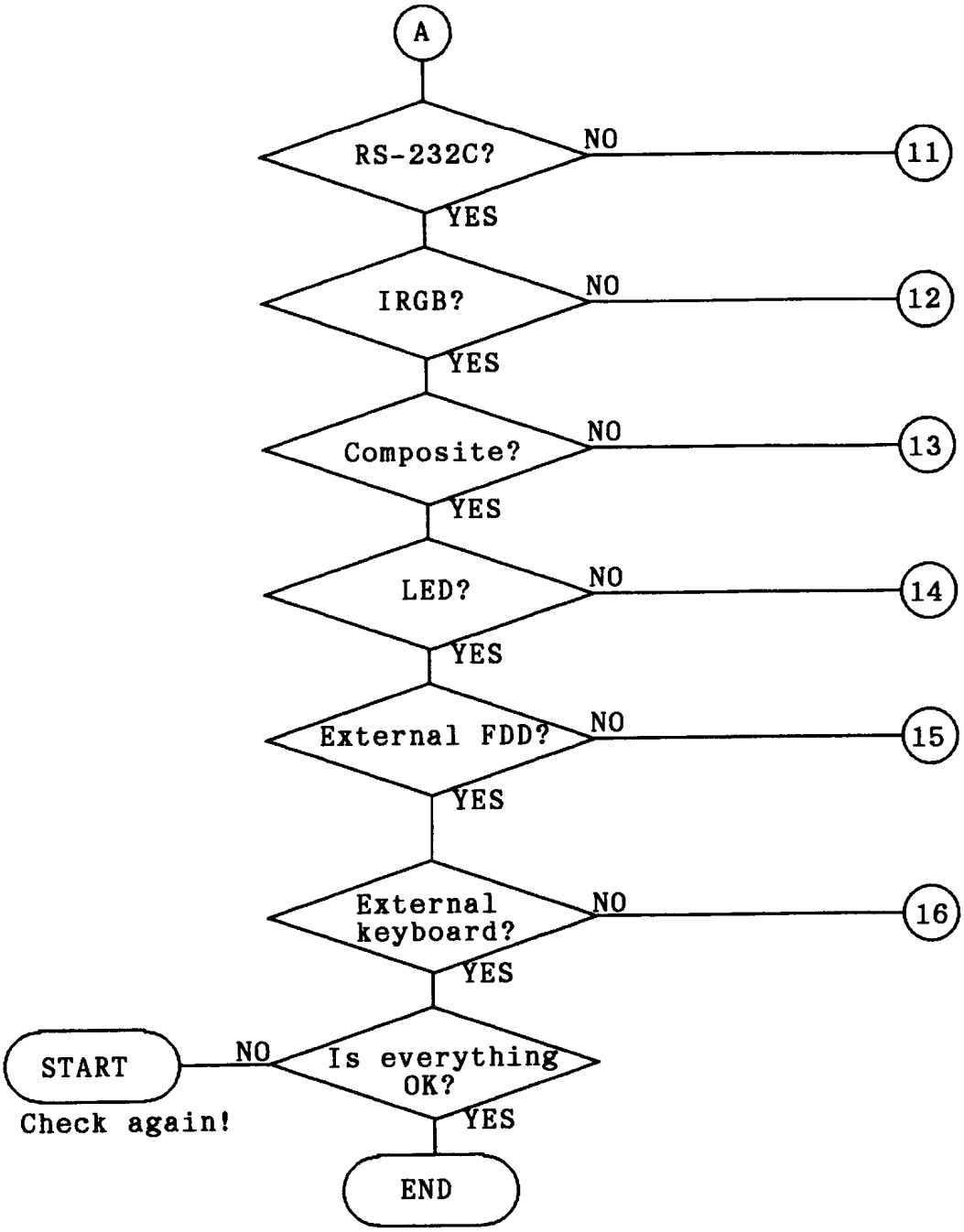
± 0.2

STEEL, ZINC COATING

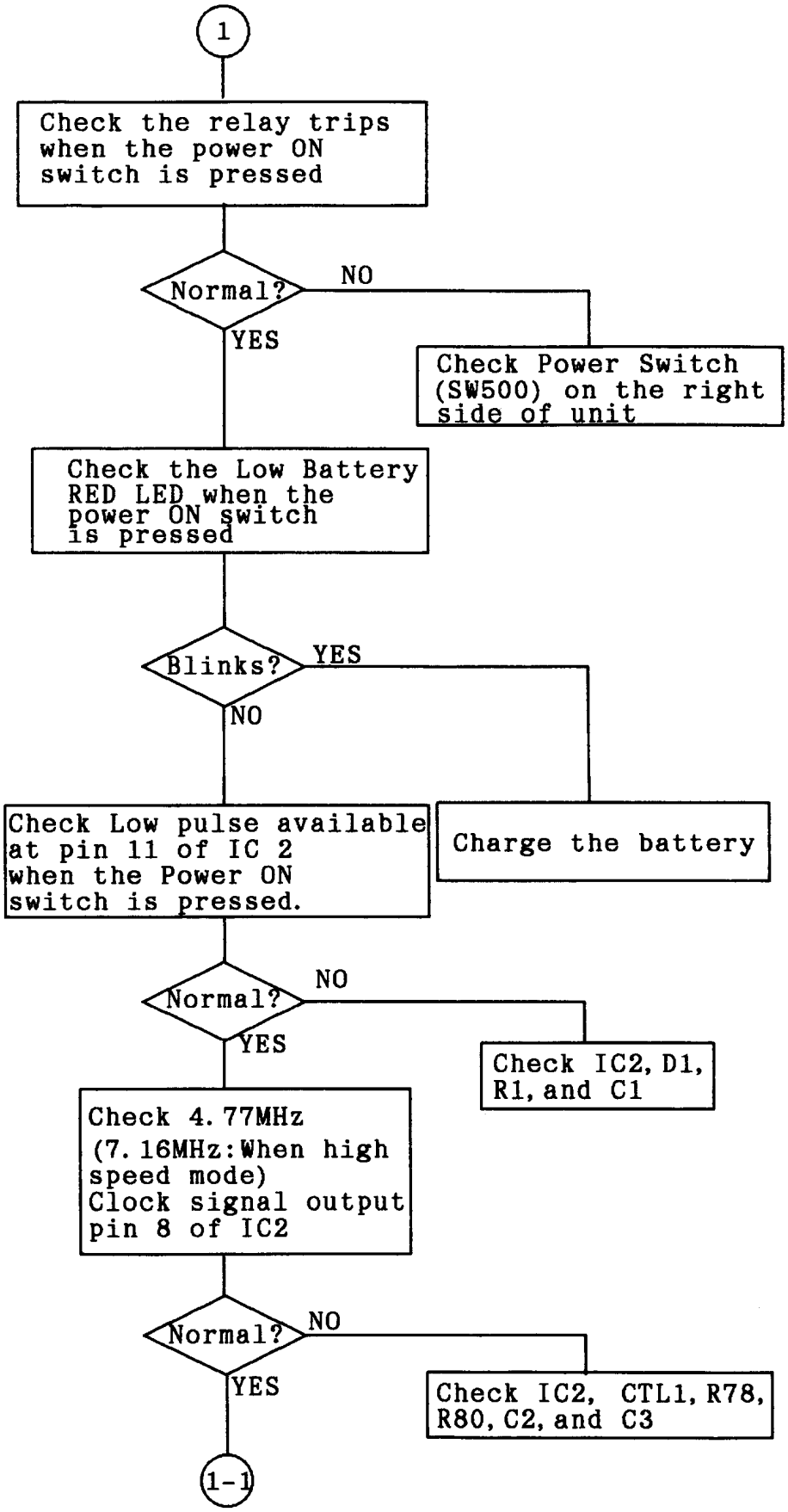
1/1 mm
1/1

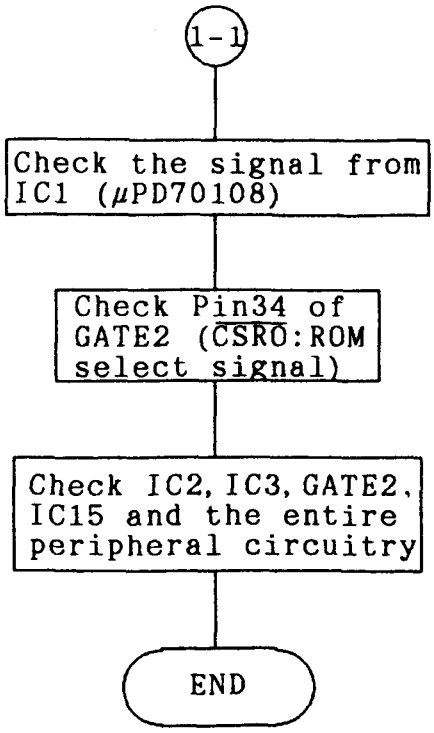
V. TROUBLESHOOTING





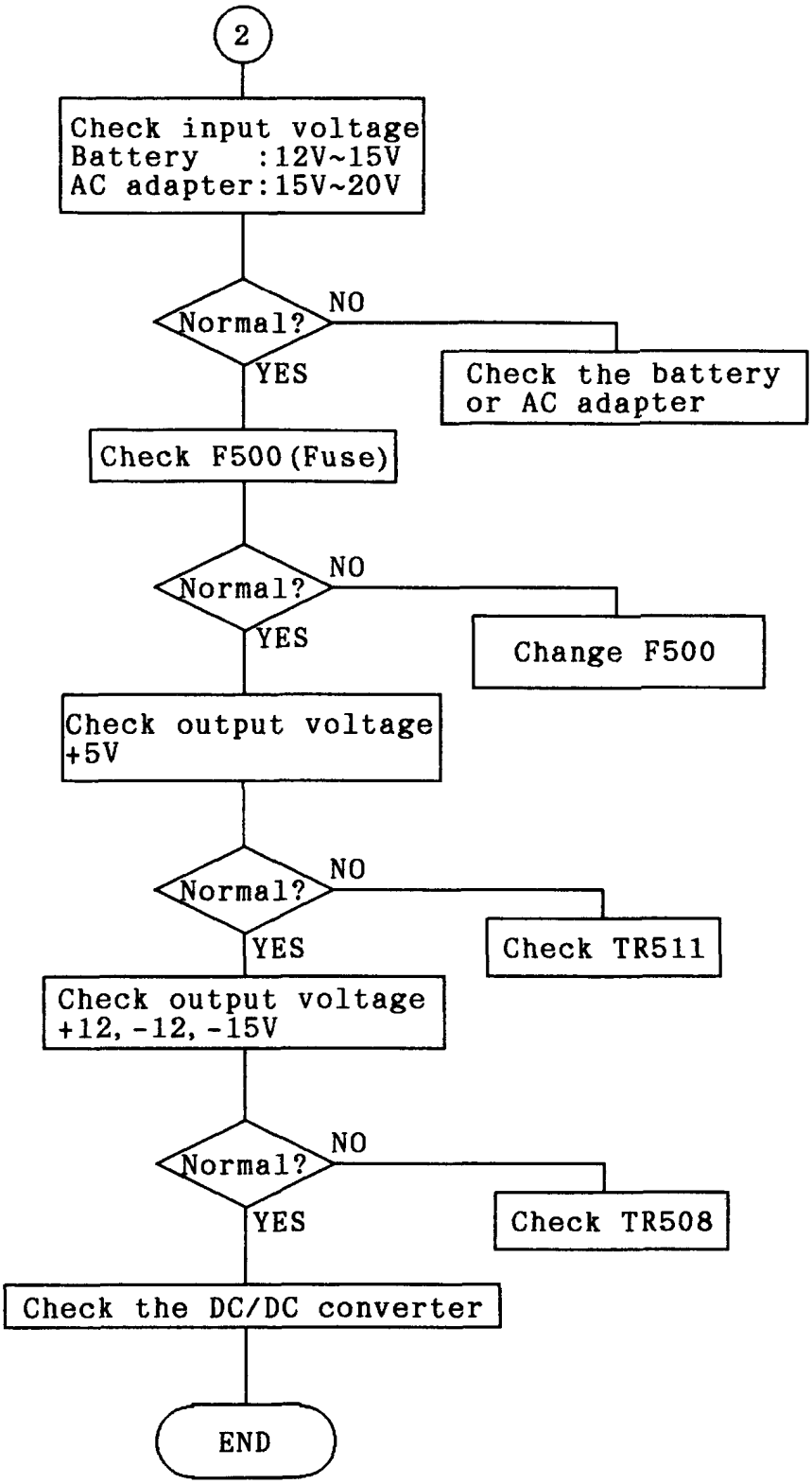
① Will Not Start



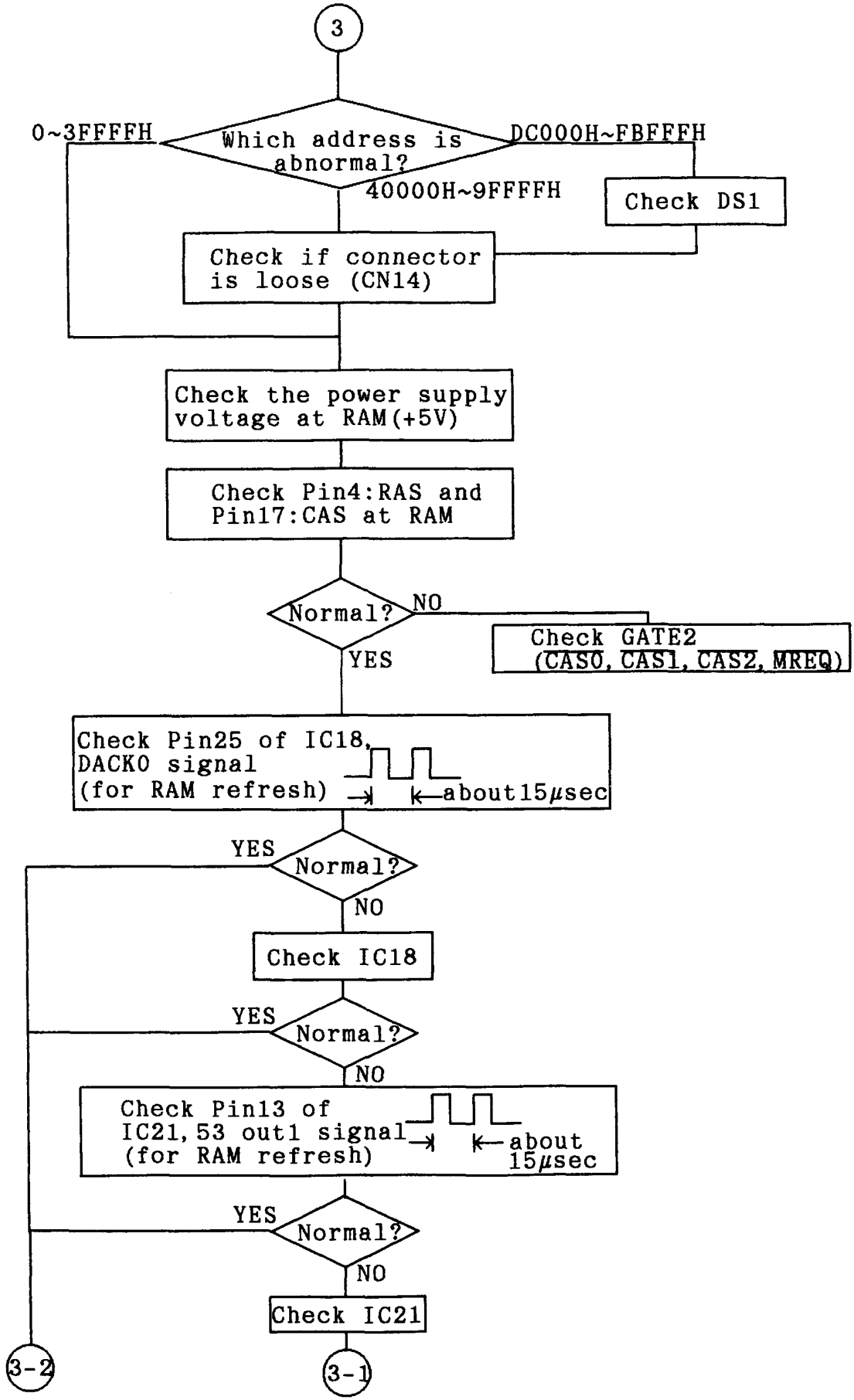


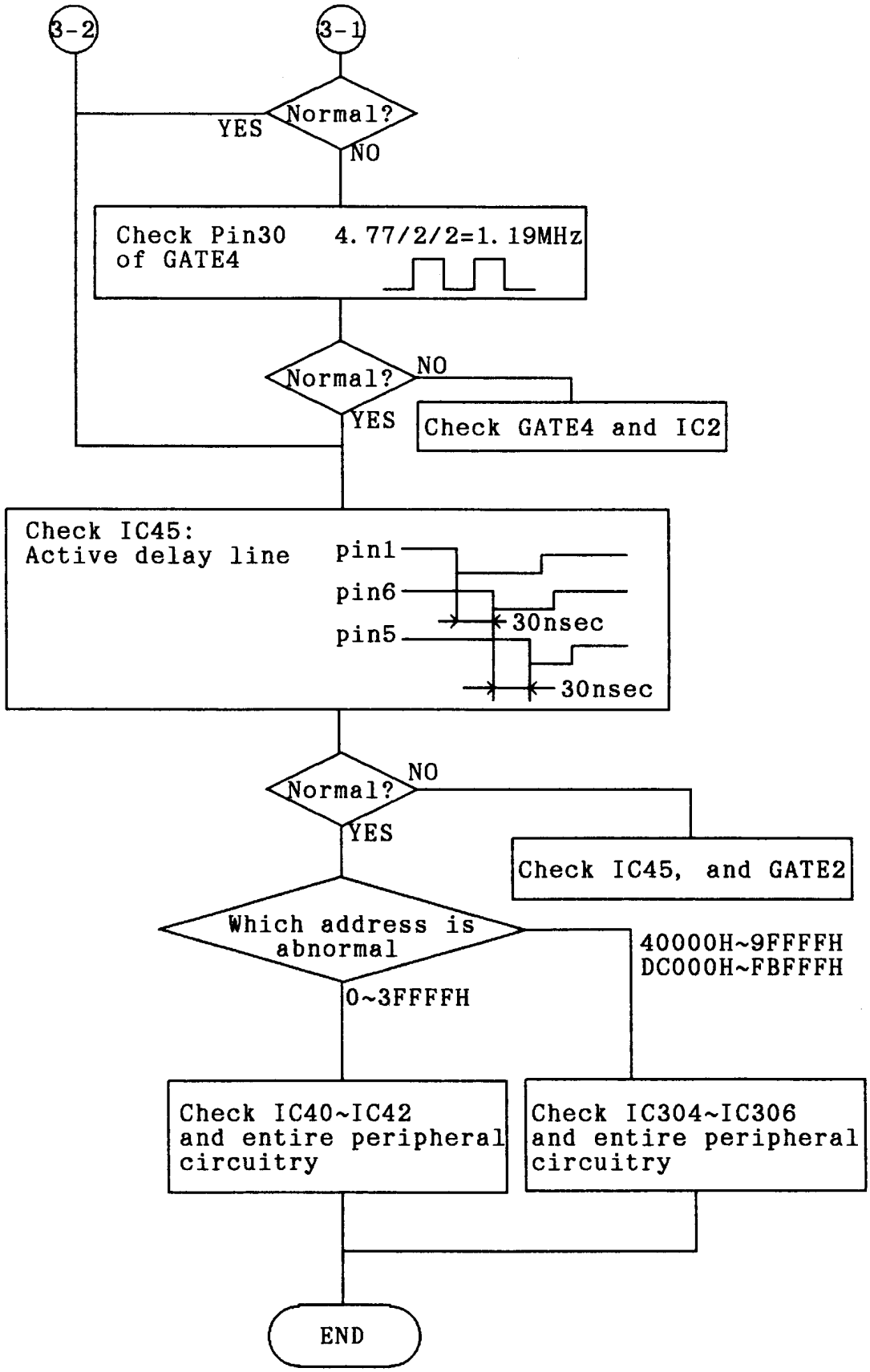
* If you need to change ROM(IC15), please peel off the copyright seal on the top of ROM, and put it to a new ROM(IC15)

② DC/DC Converter Check

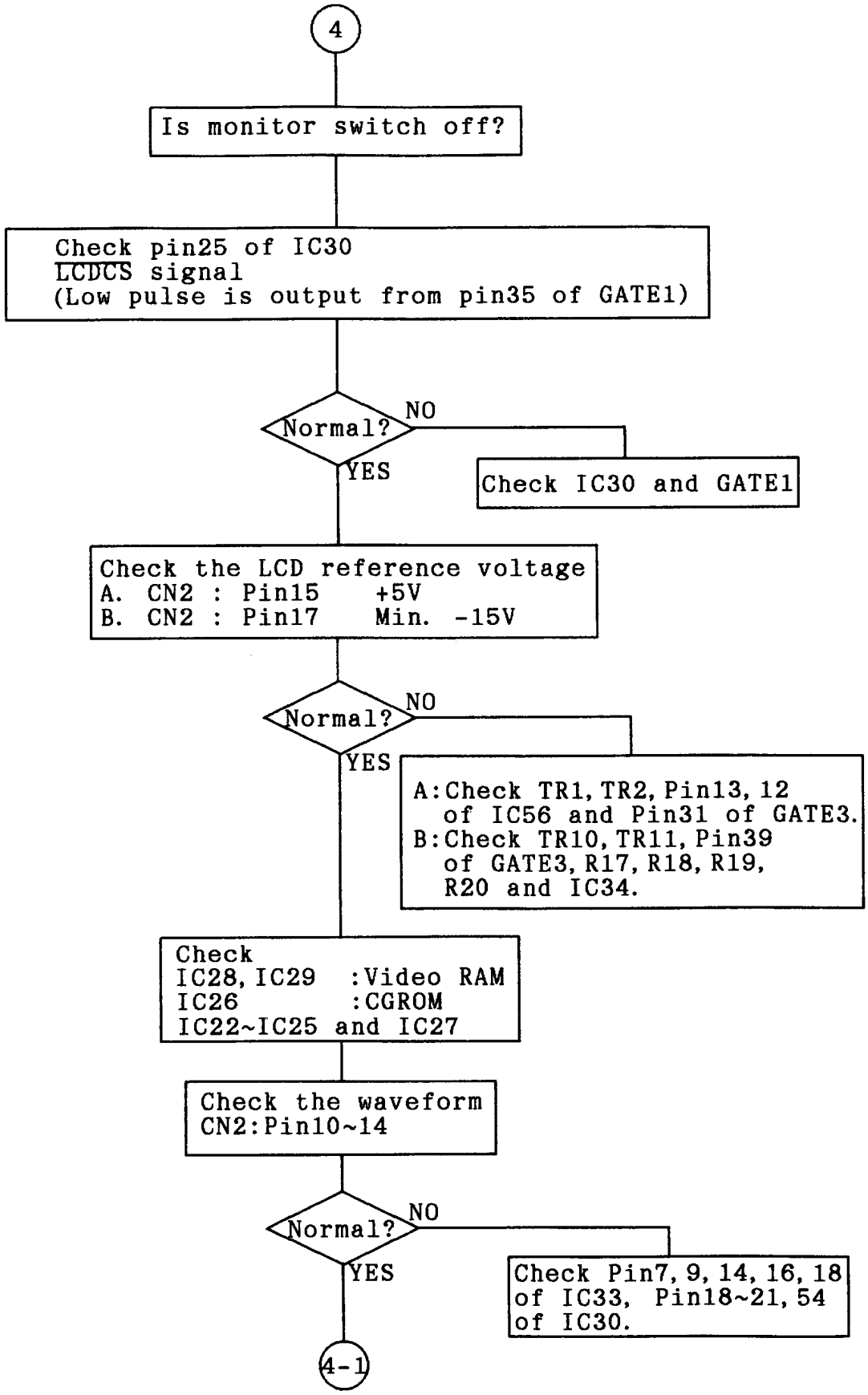


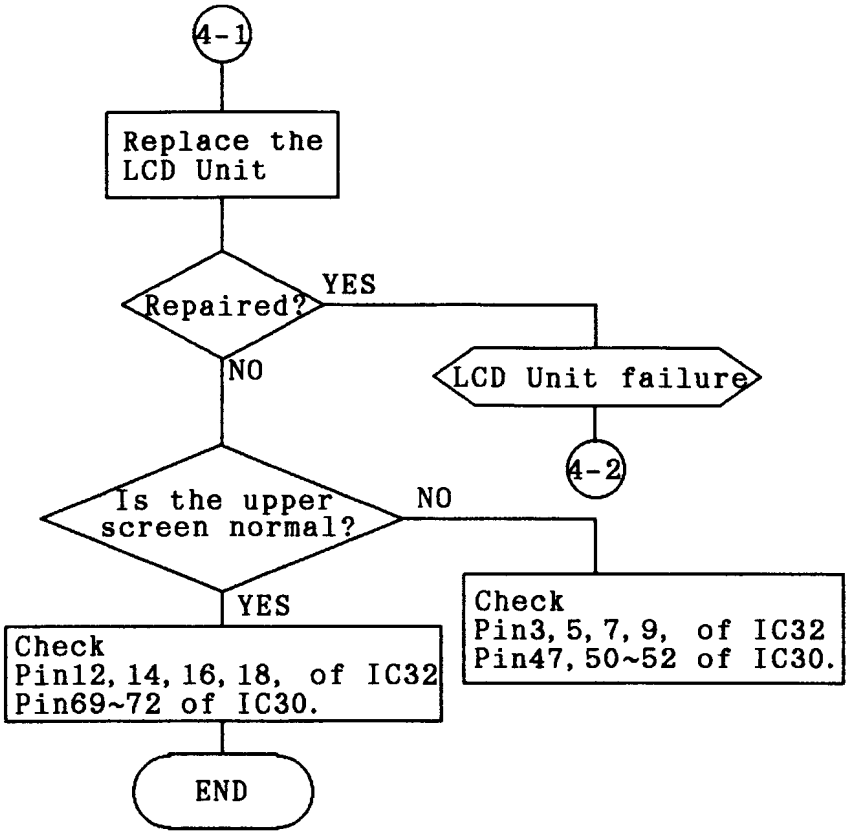
③ Memory Check



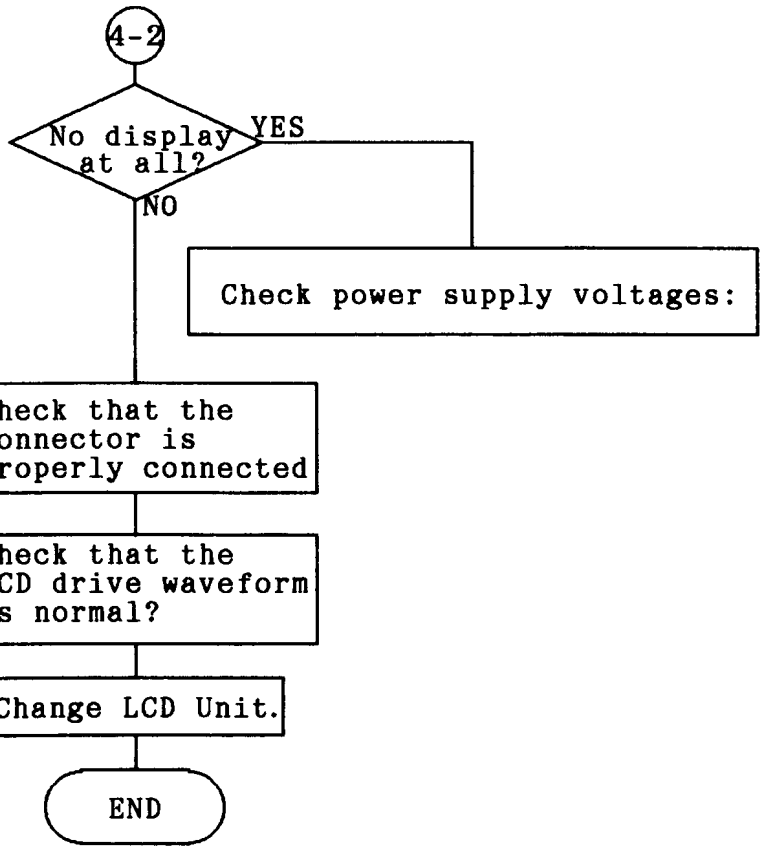


④ LCD Check

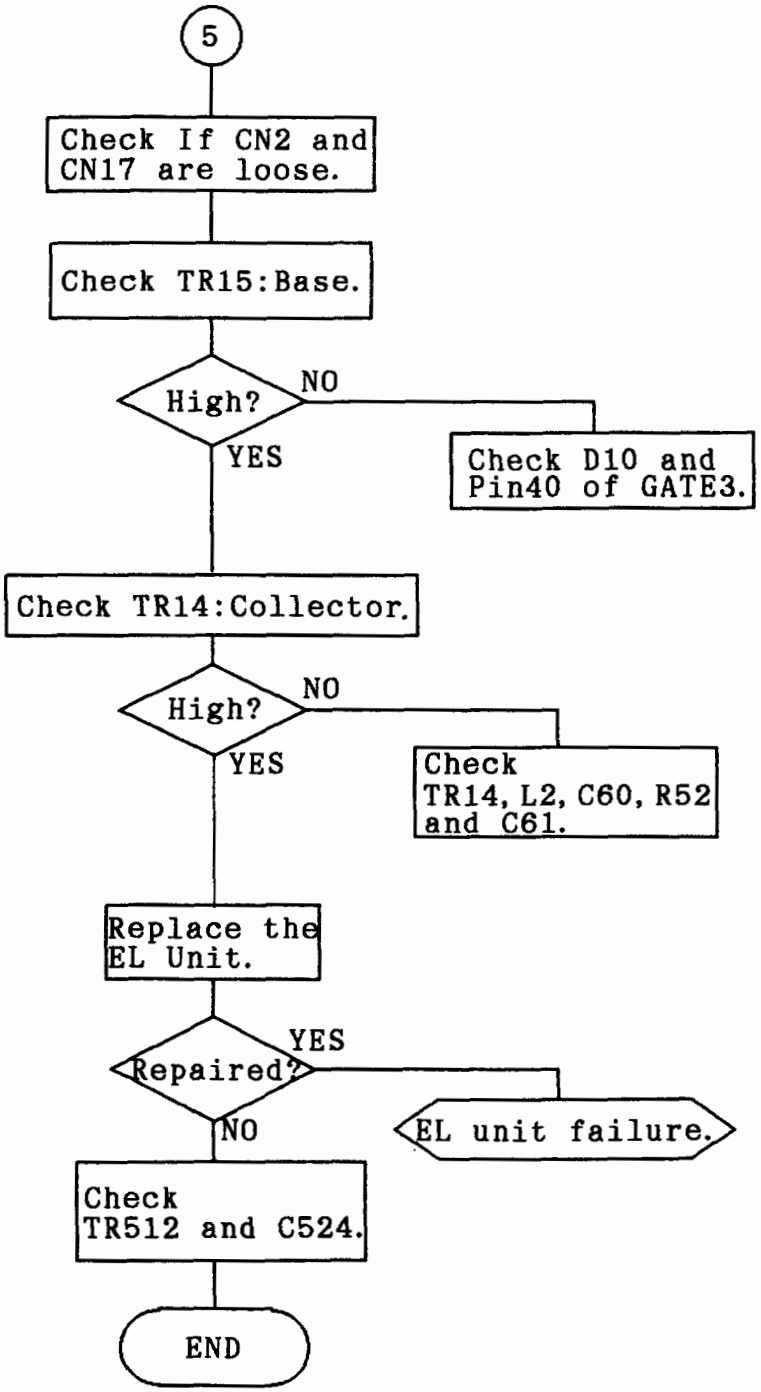




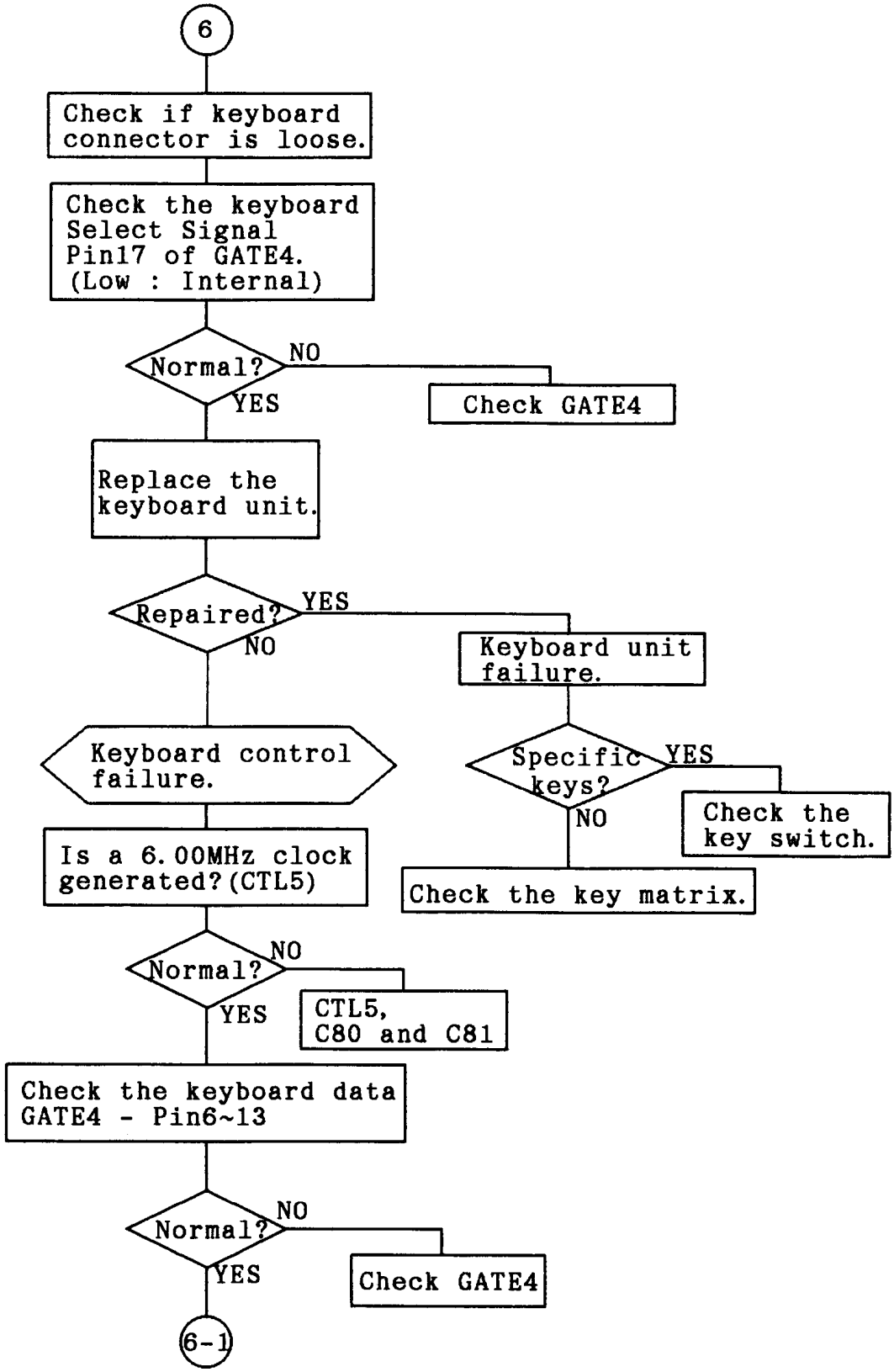
LCD unit

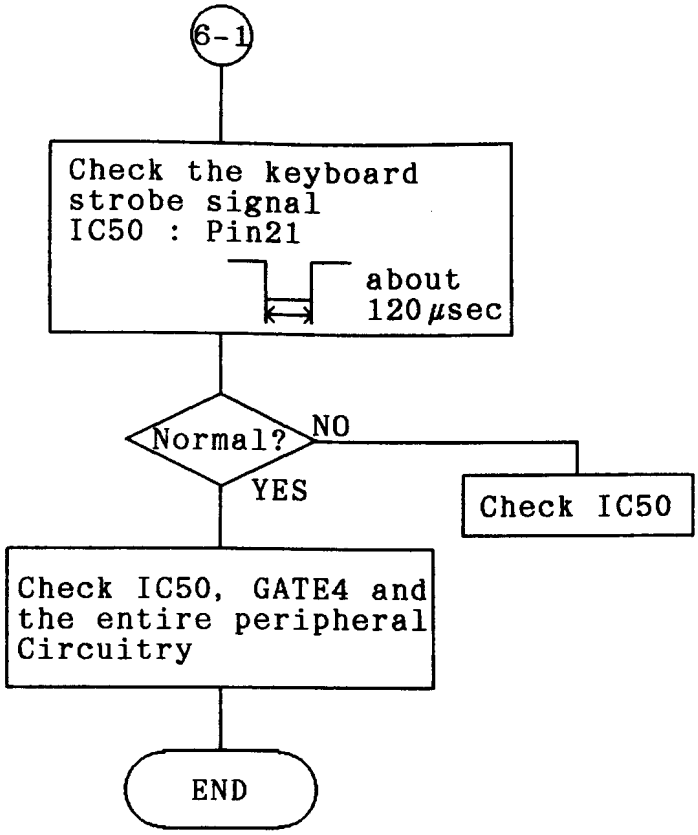


⑤ EL Check

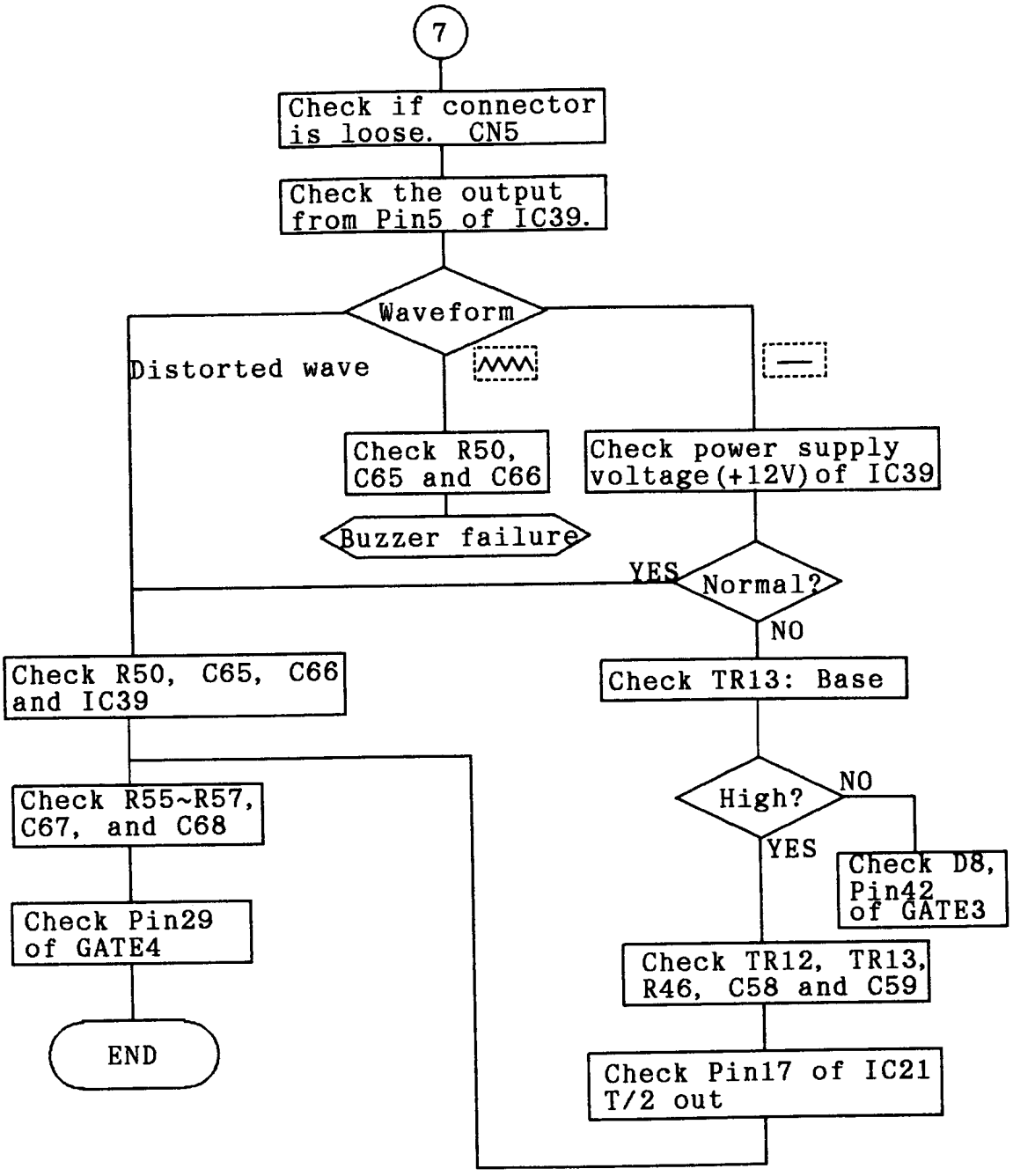


⑥ Internal Keyboard Check

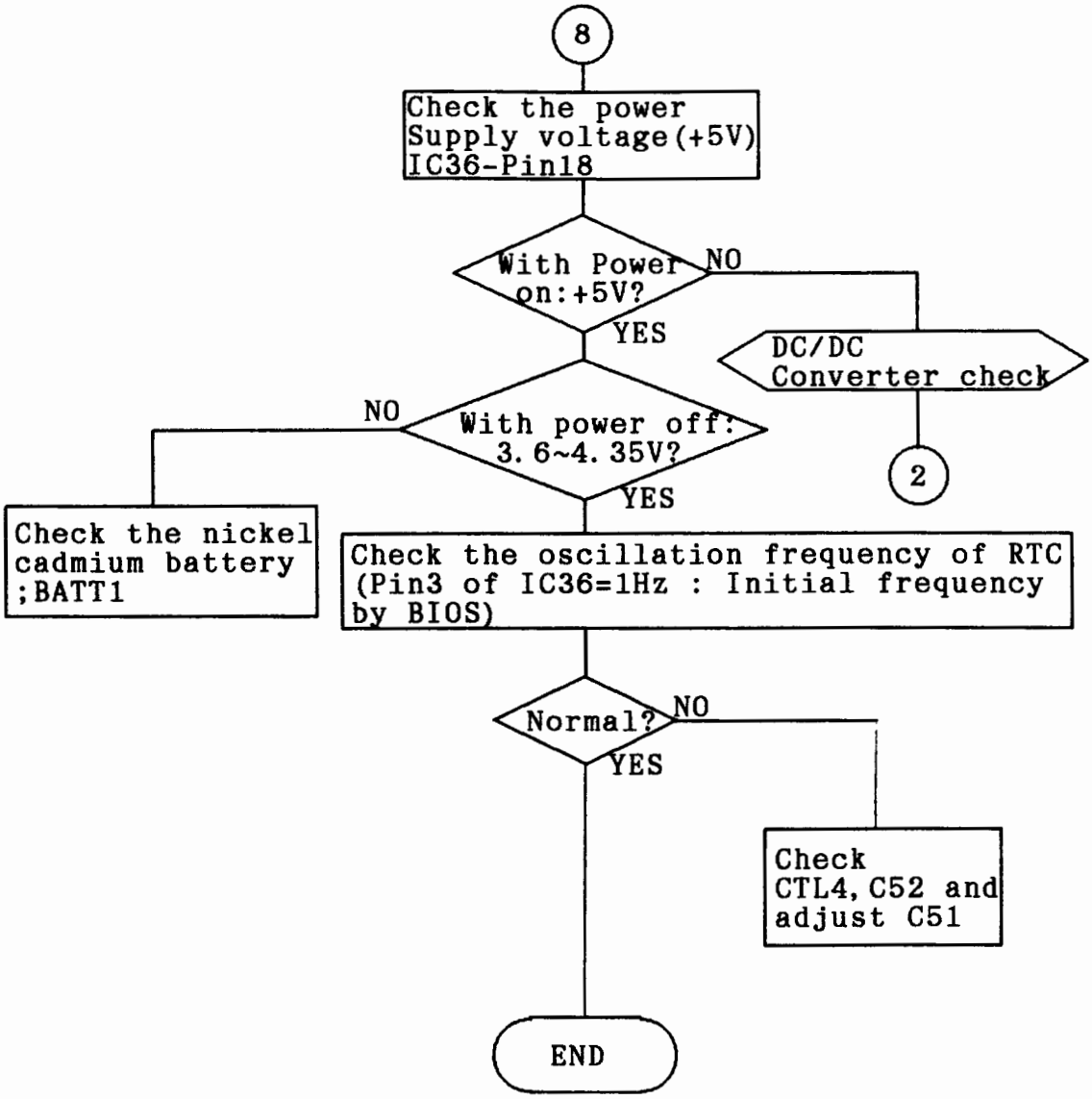




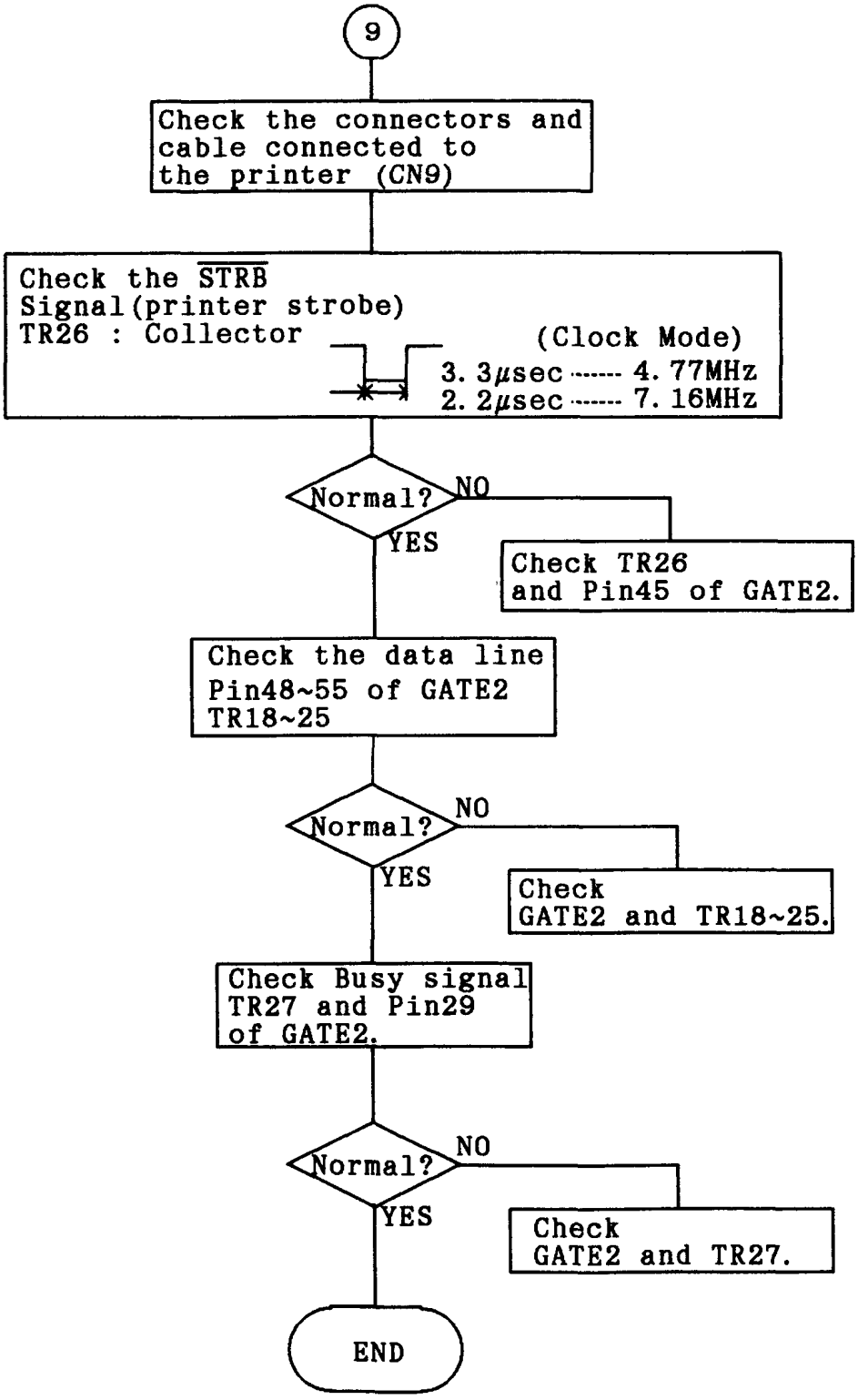
⑦ Buzzer Check



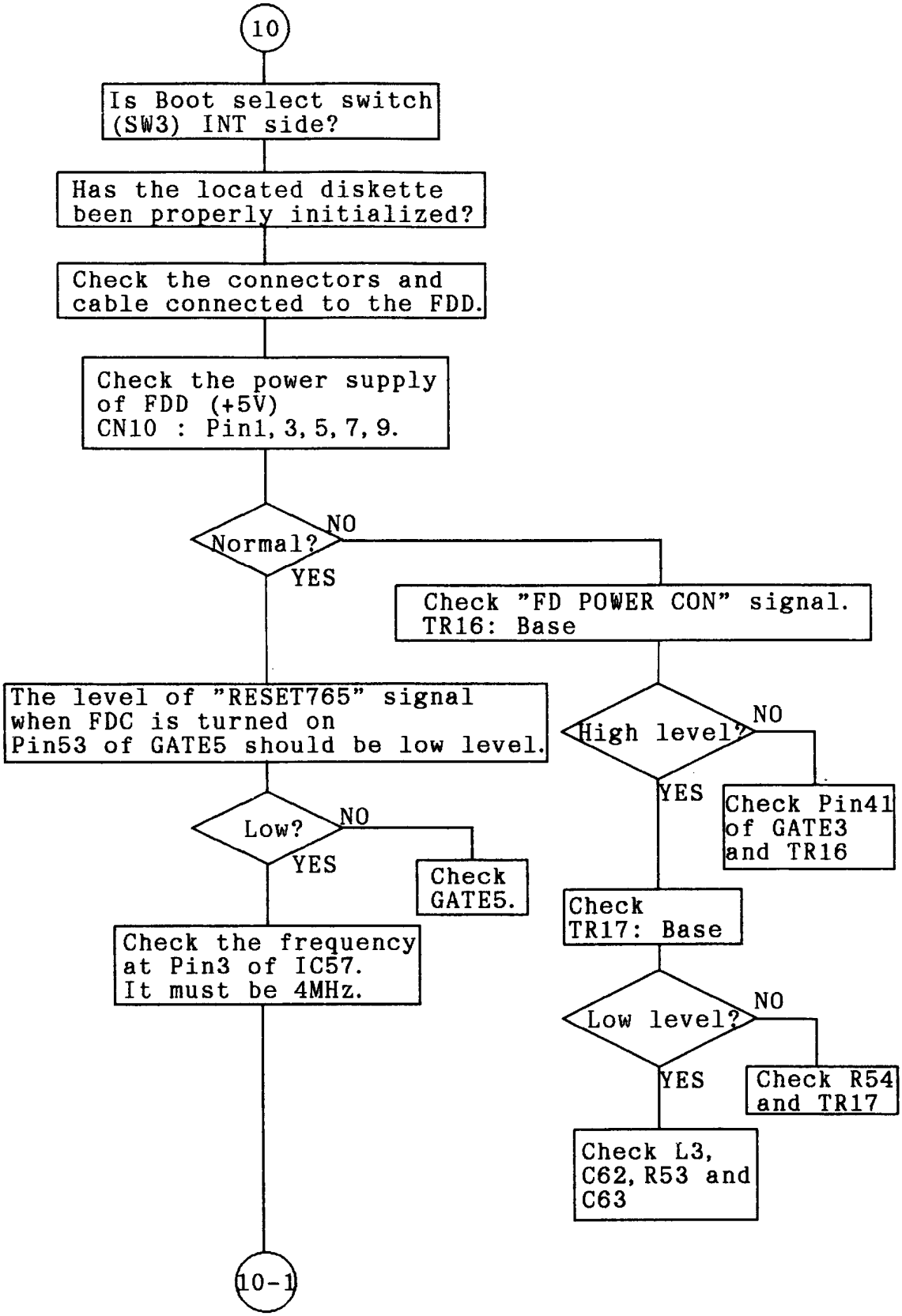
⑧ RTC (Real-Time Clock) Check

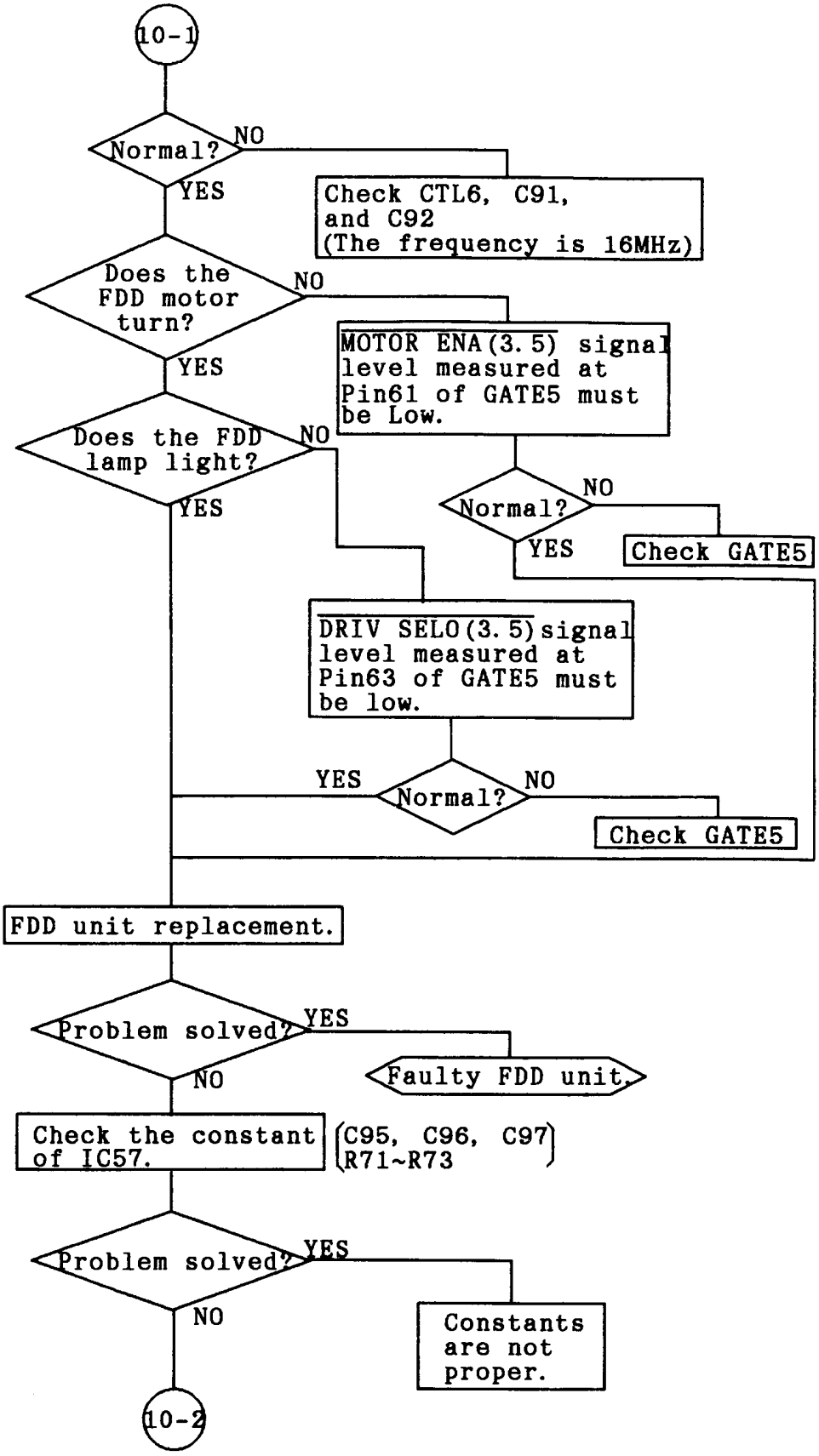


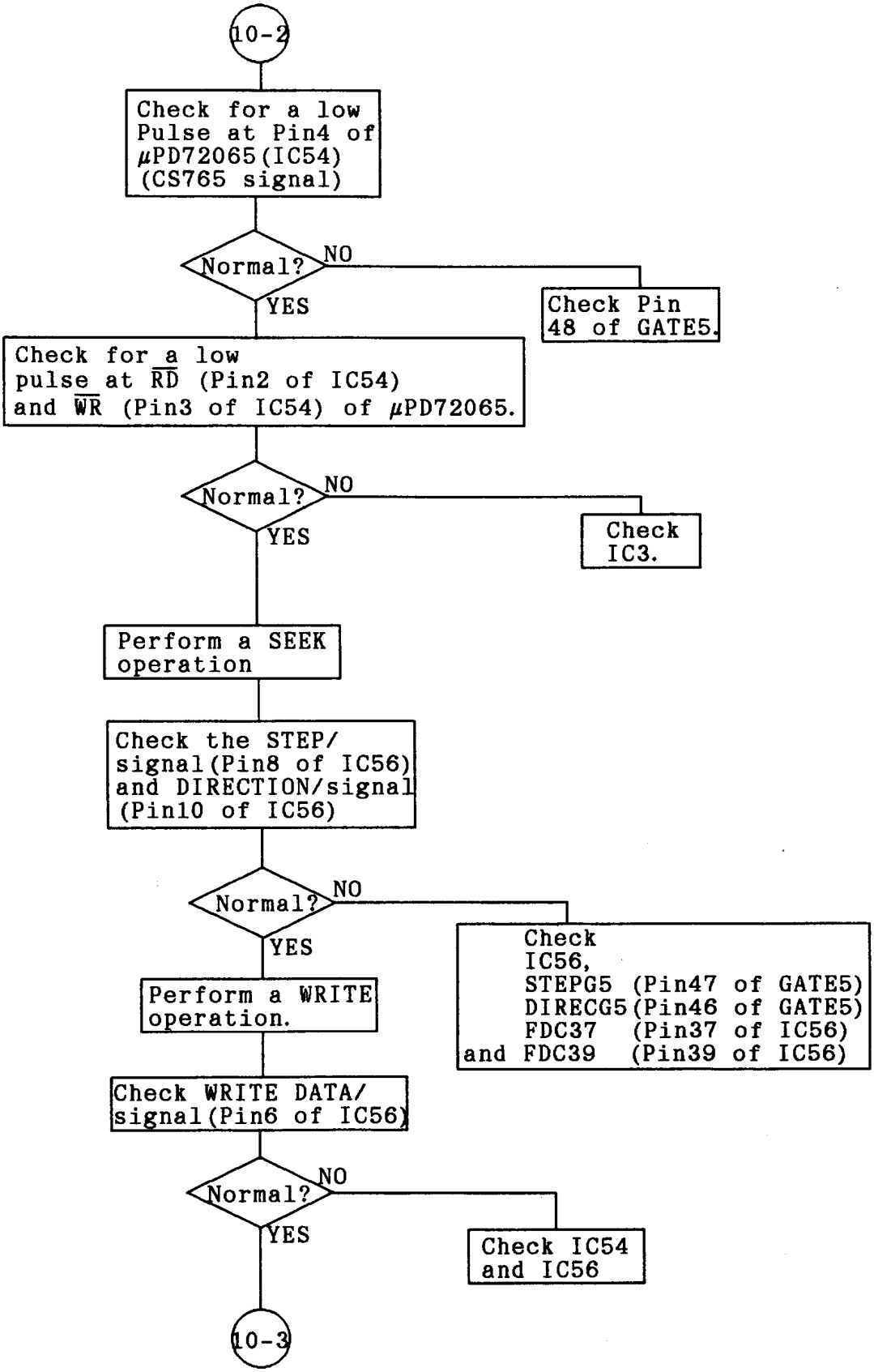
⑨ Printer Interface

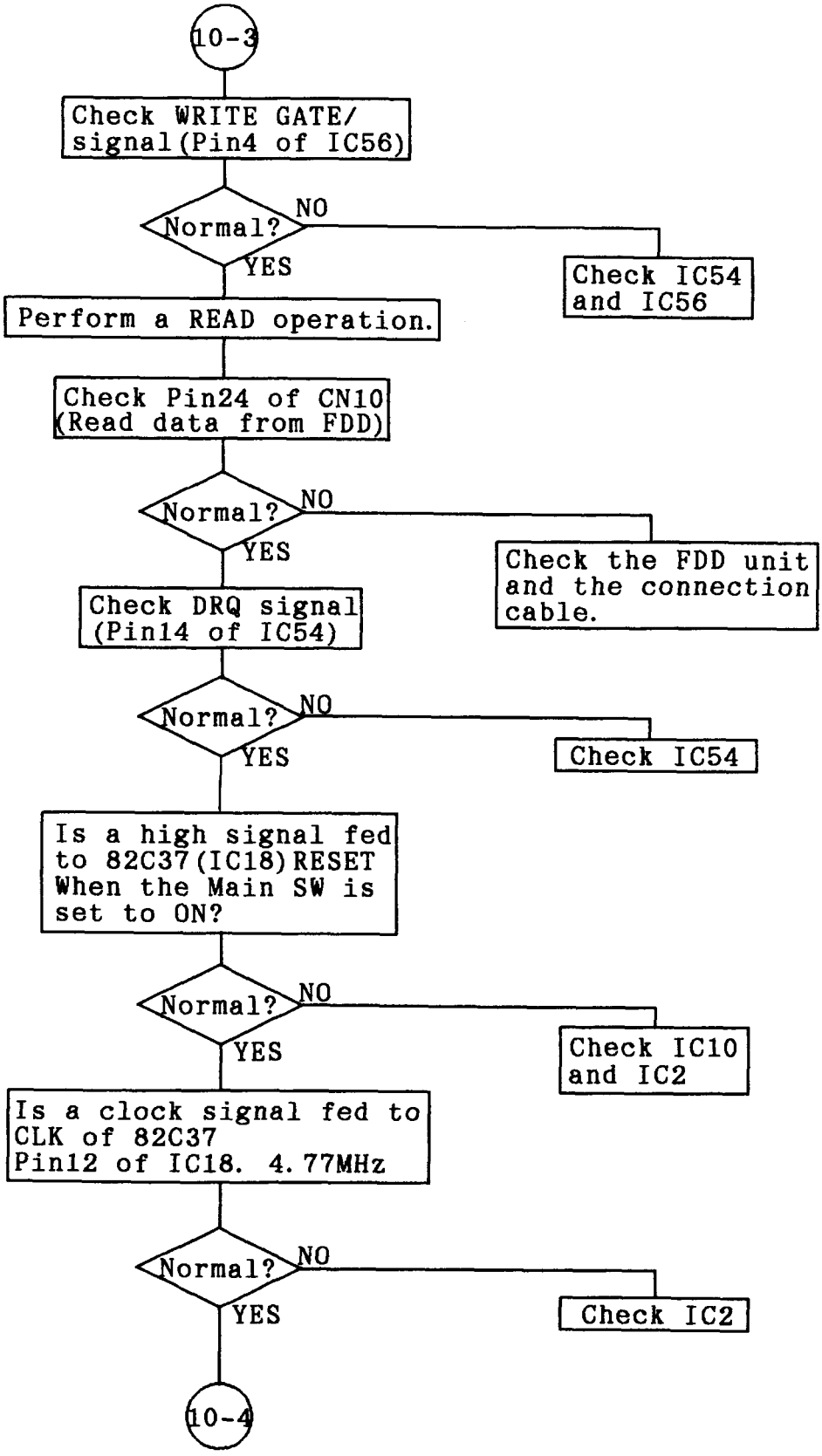


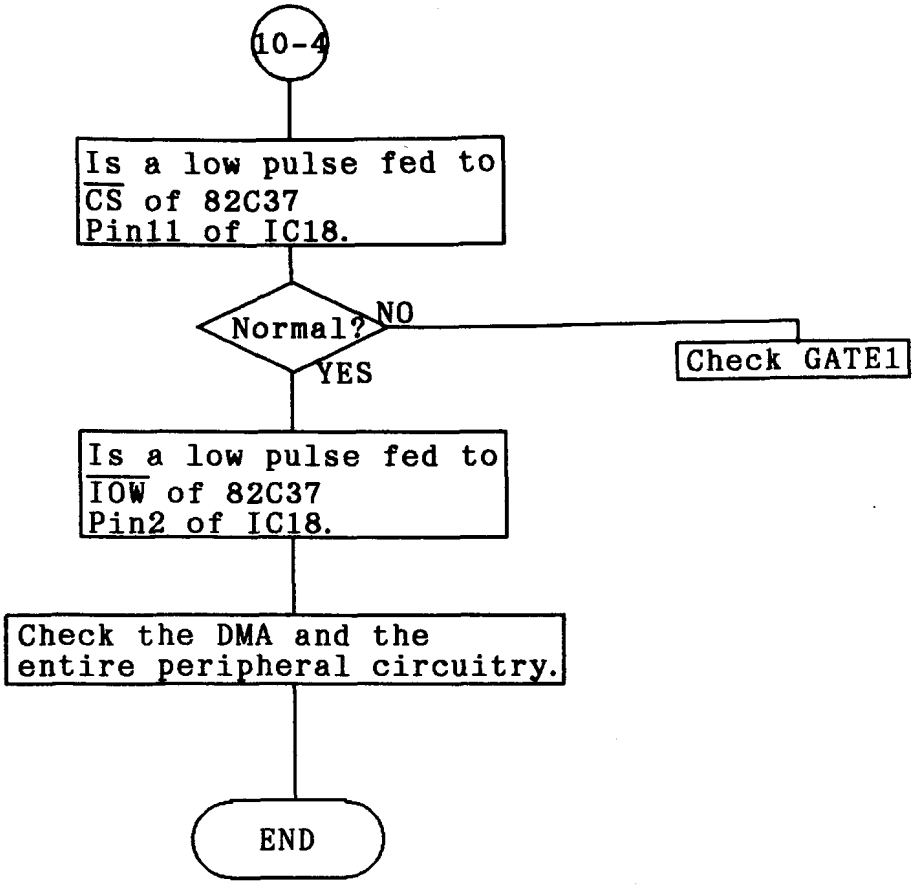
⑩ Internal FDD Troubleshooting



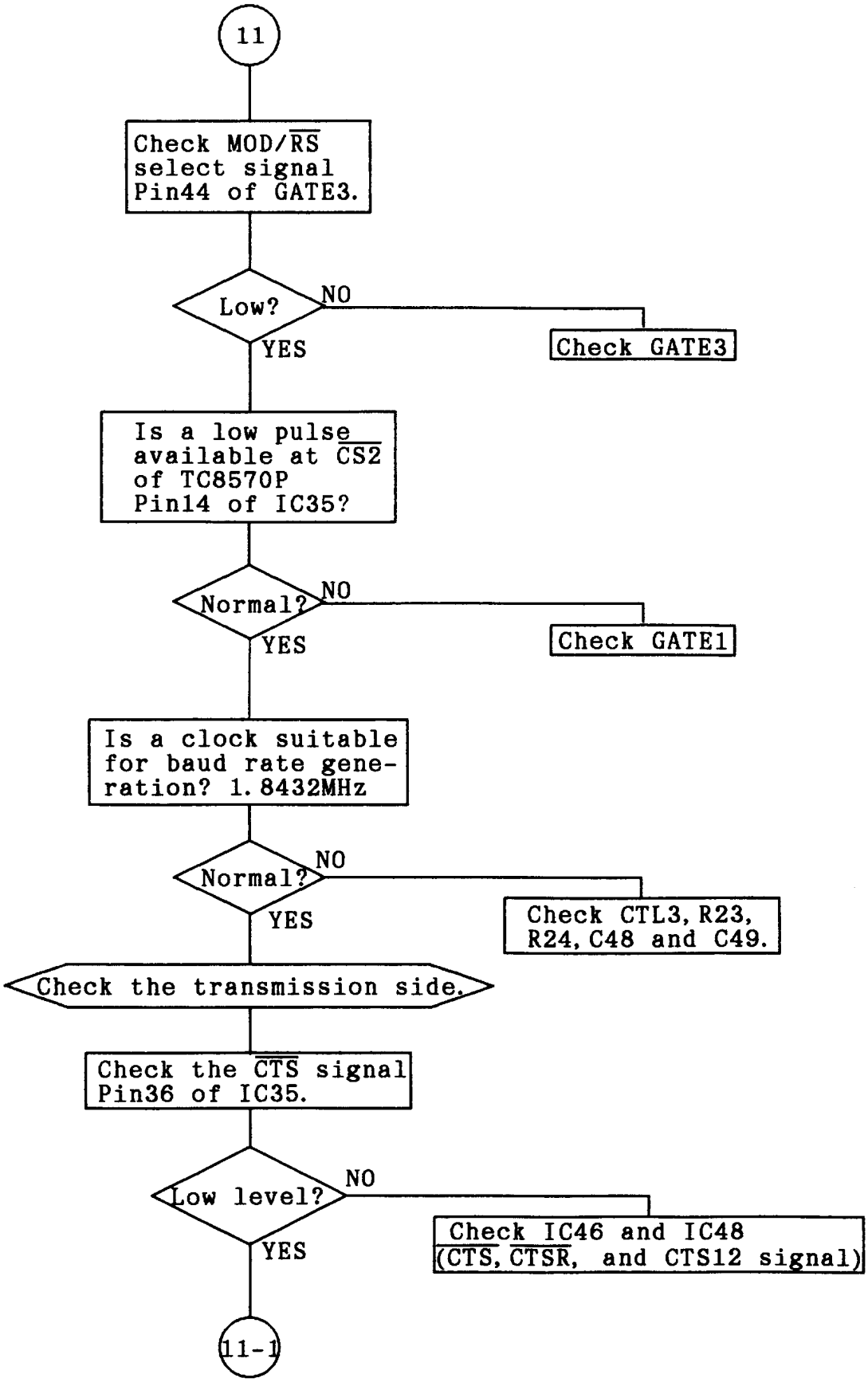


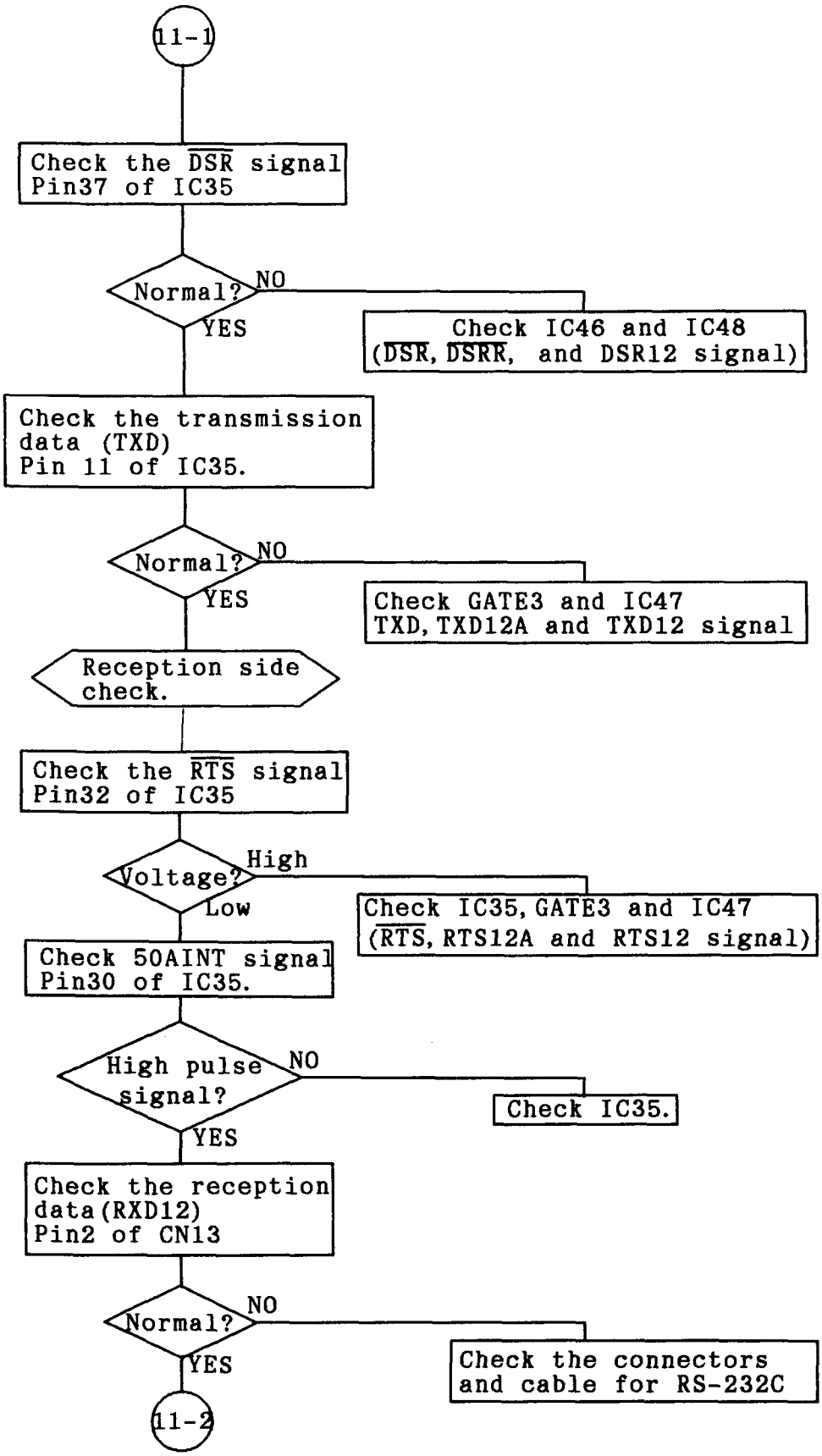


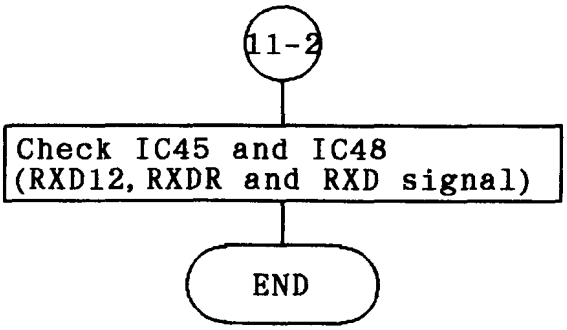




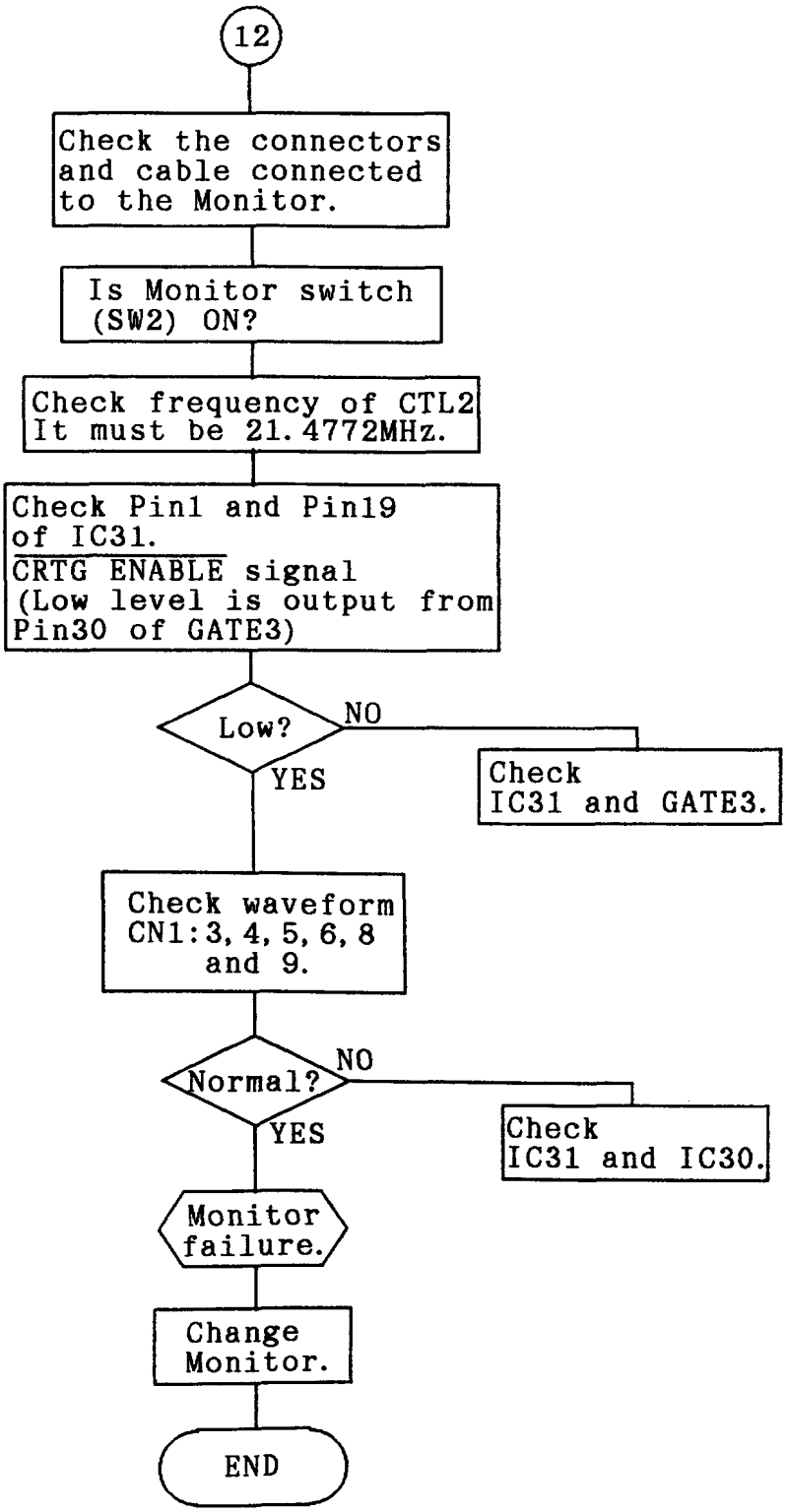
⑪ RS-232C Check



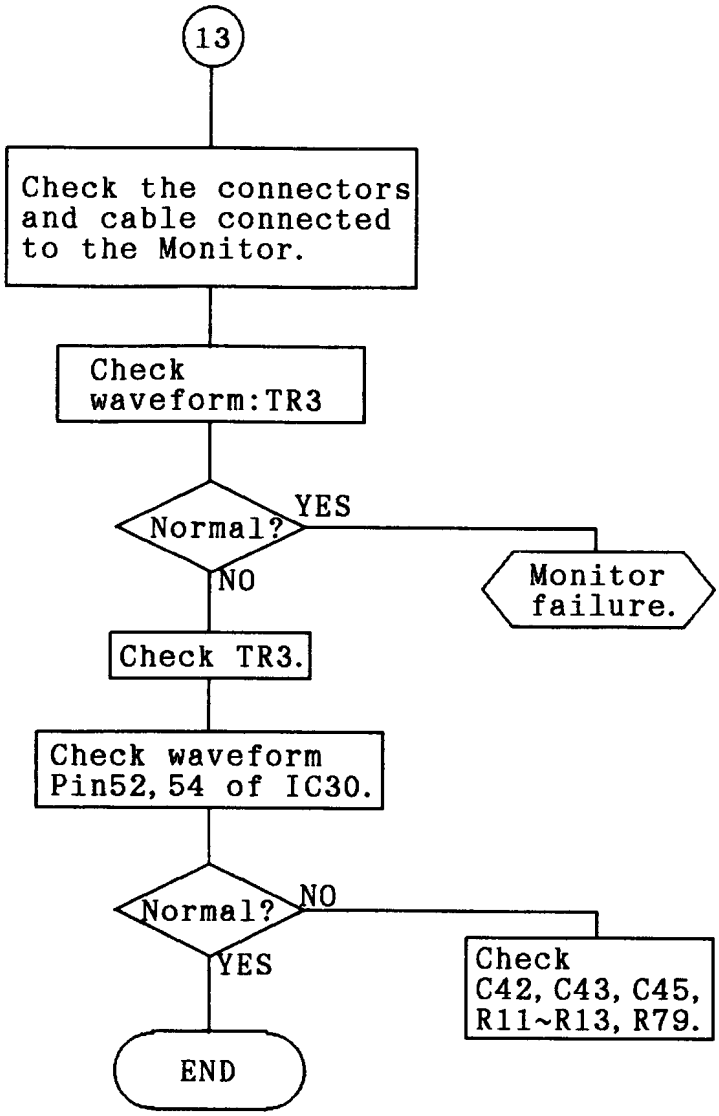




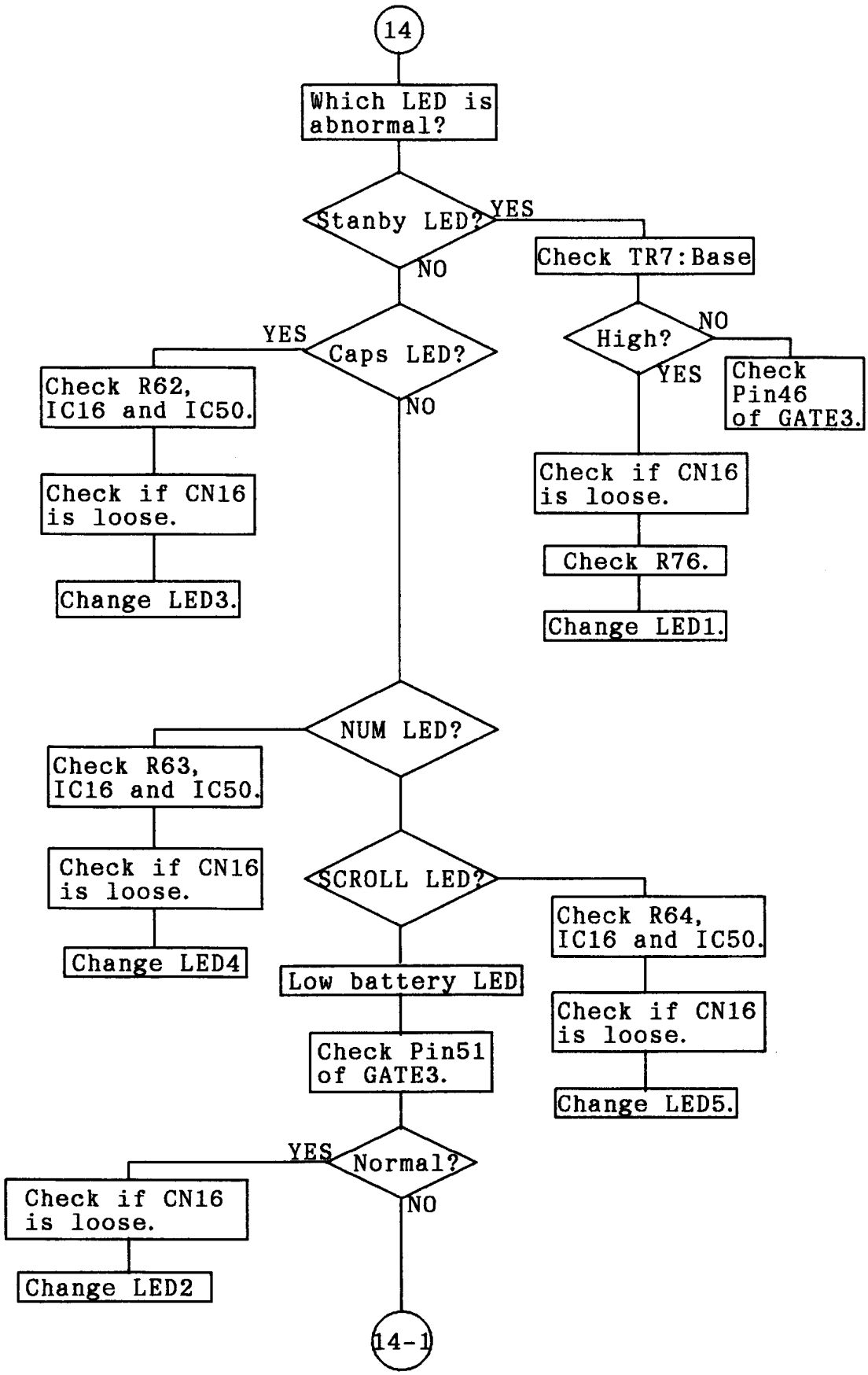
⑫ IRGB Check

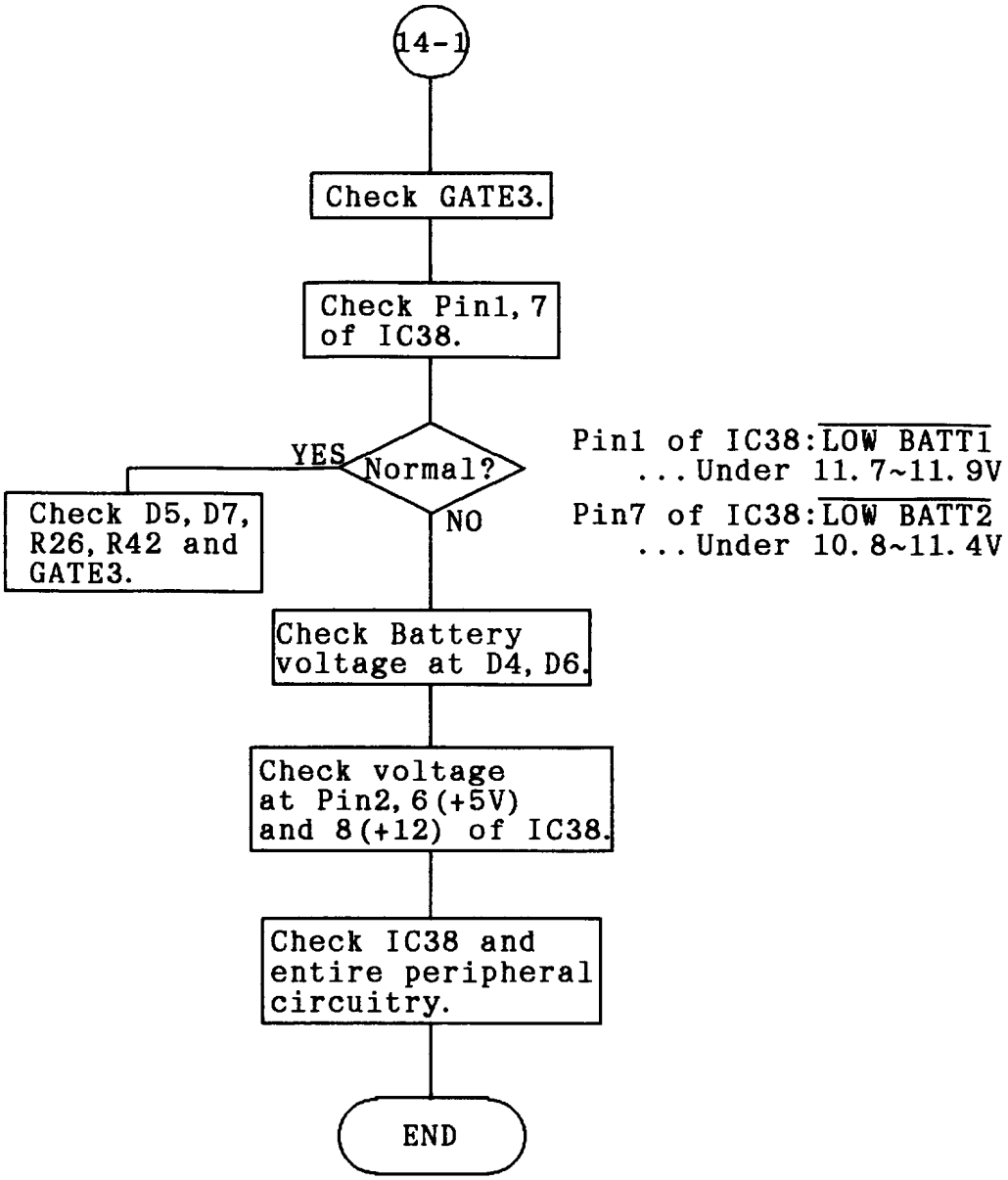


⑬ Composite CRT Check

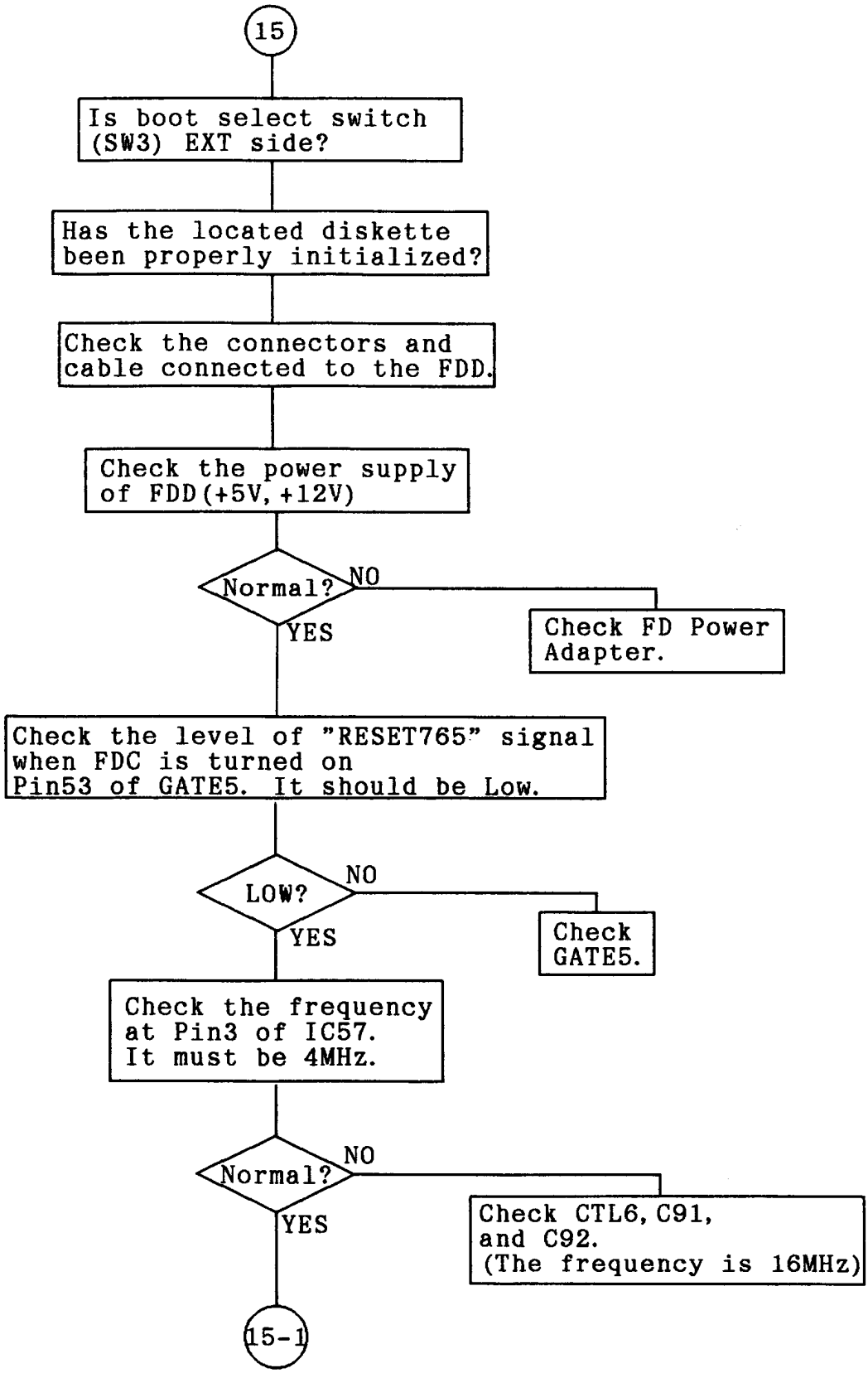


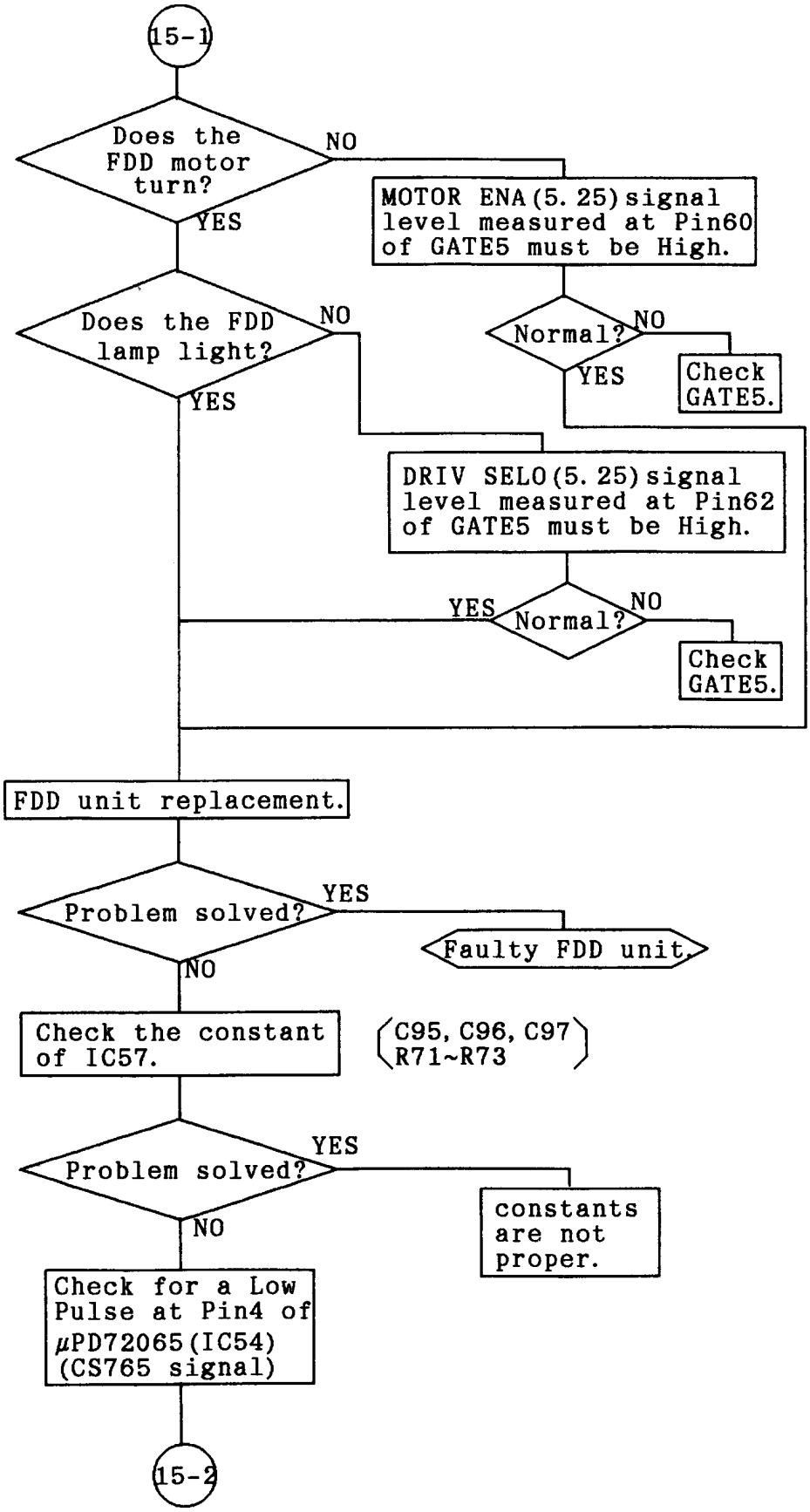
⑭ LED Check

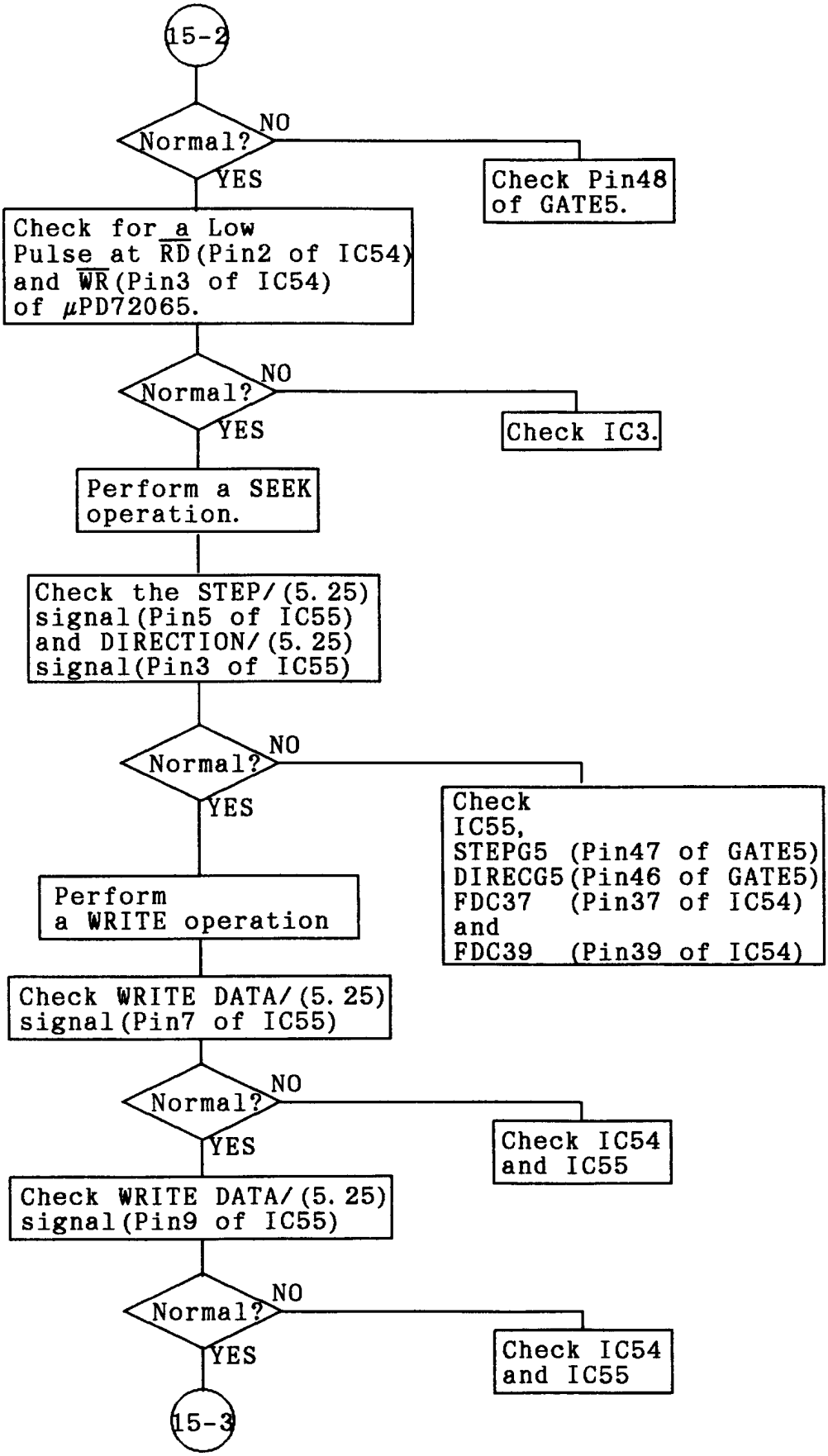


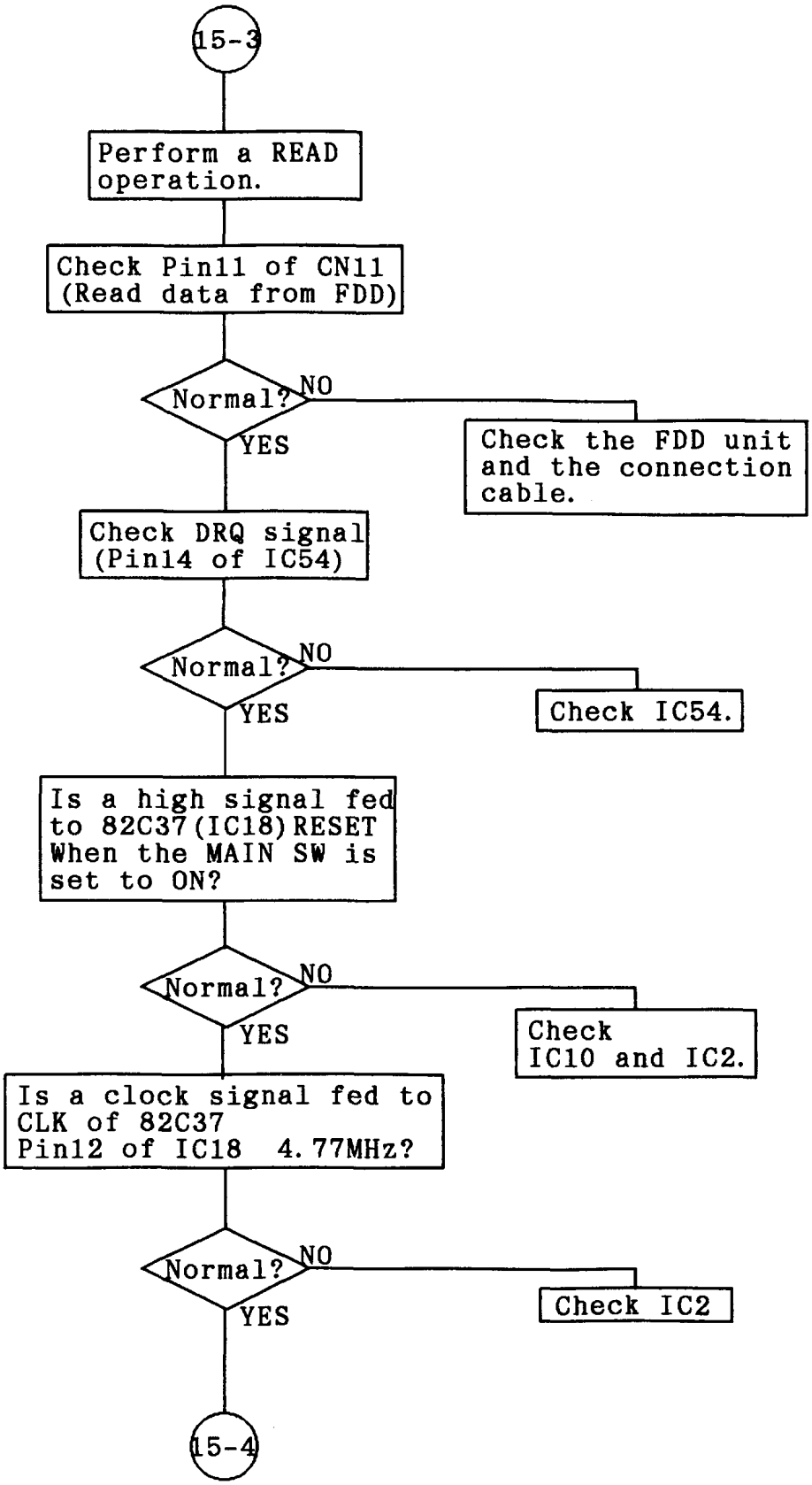


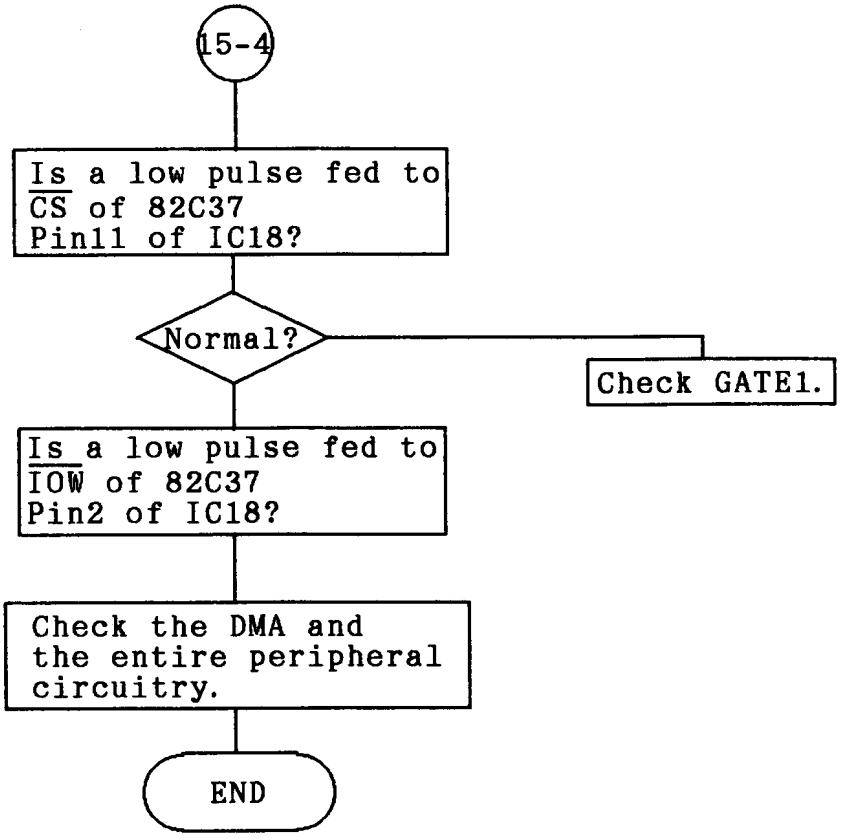
⑮ External FDD Troubleshooting



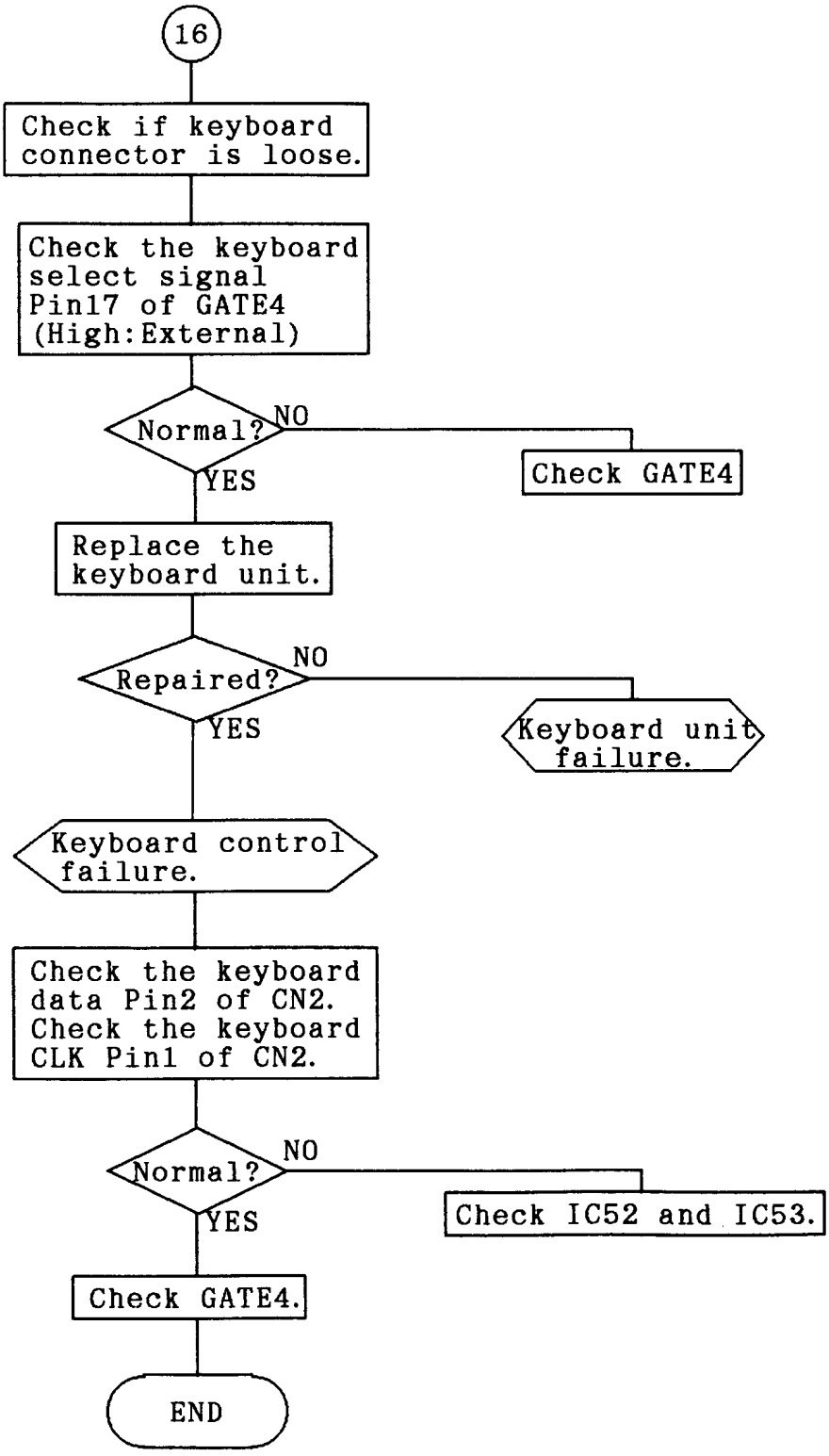








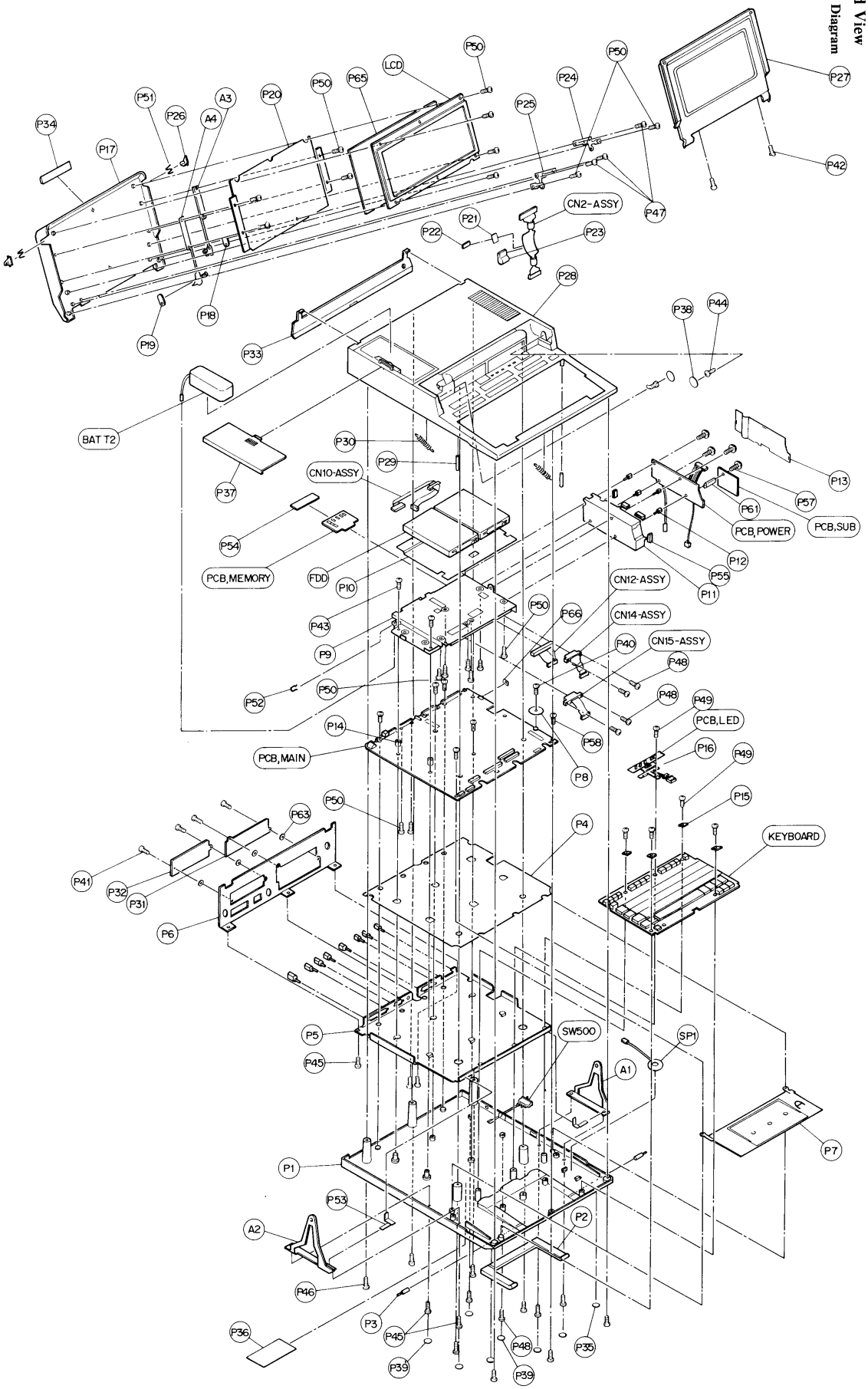
⑯ External Keyboard Check

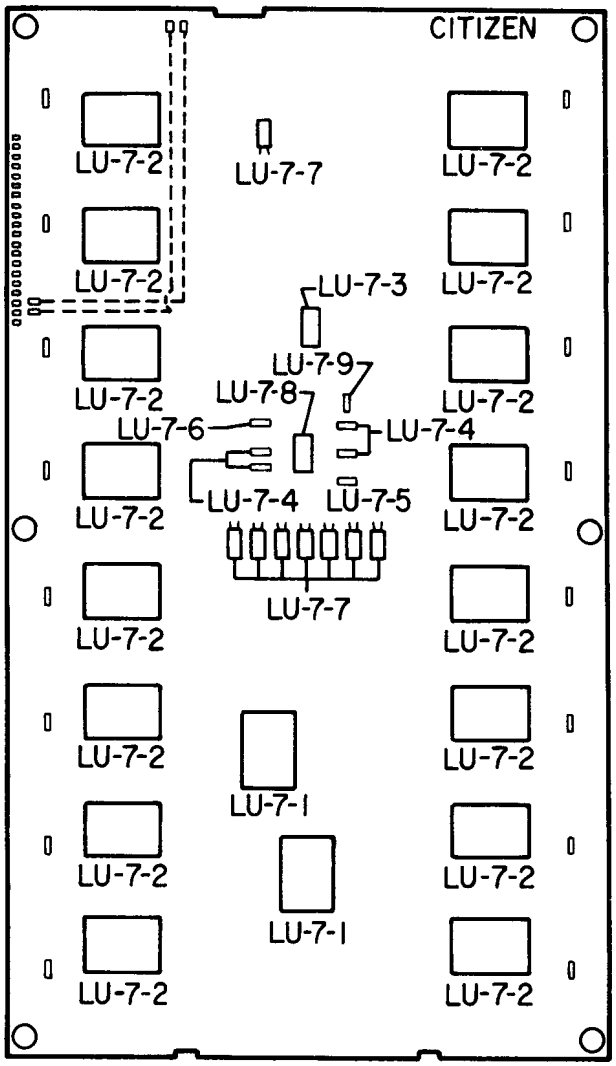


VI. EXPLODED VIEW and PARTS LIST

VI-1. Exploded View

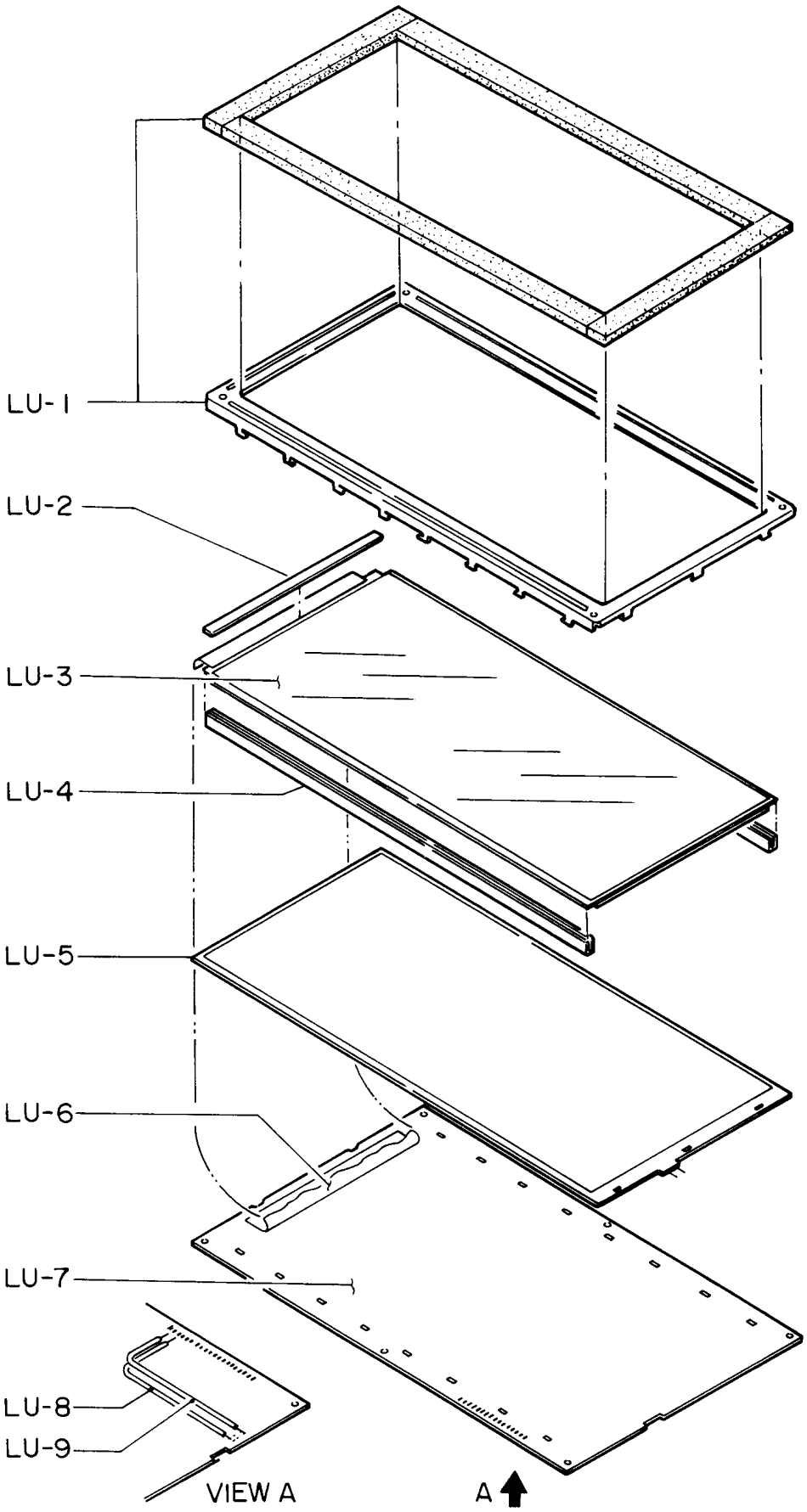
Overall Assembly Diagram



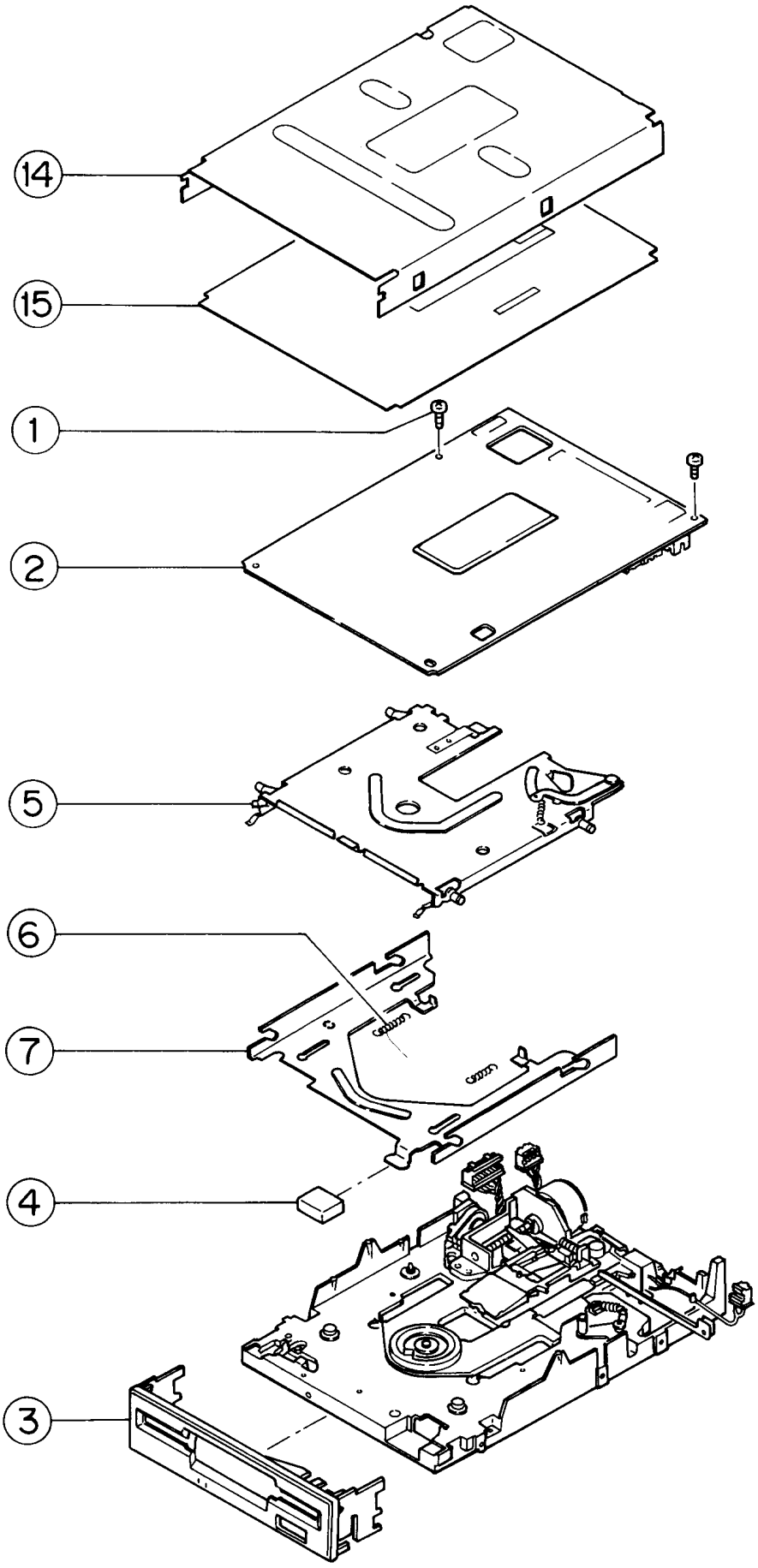


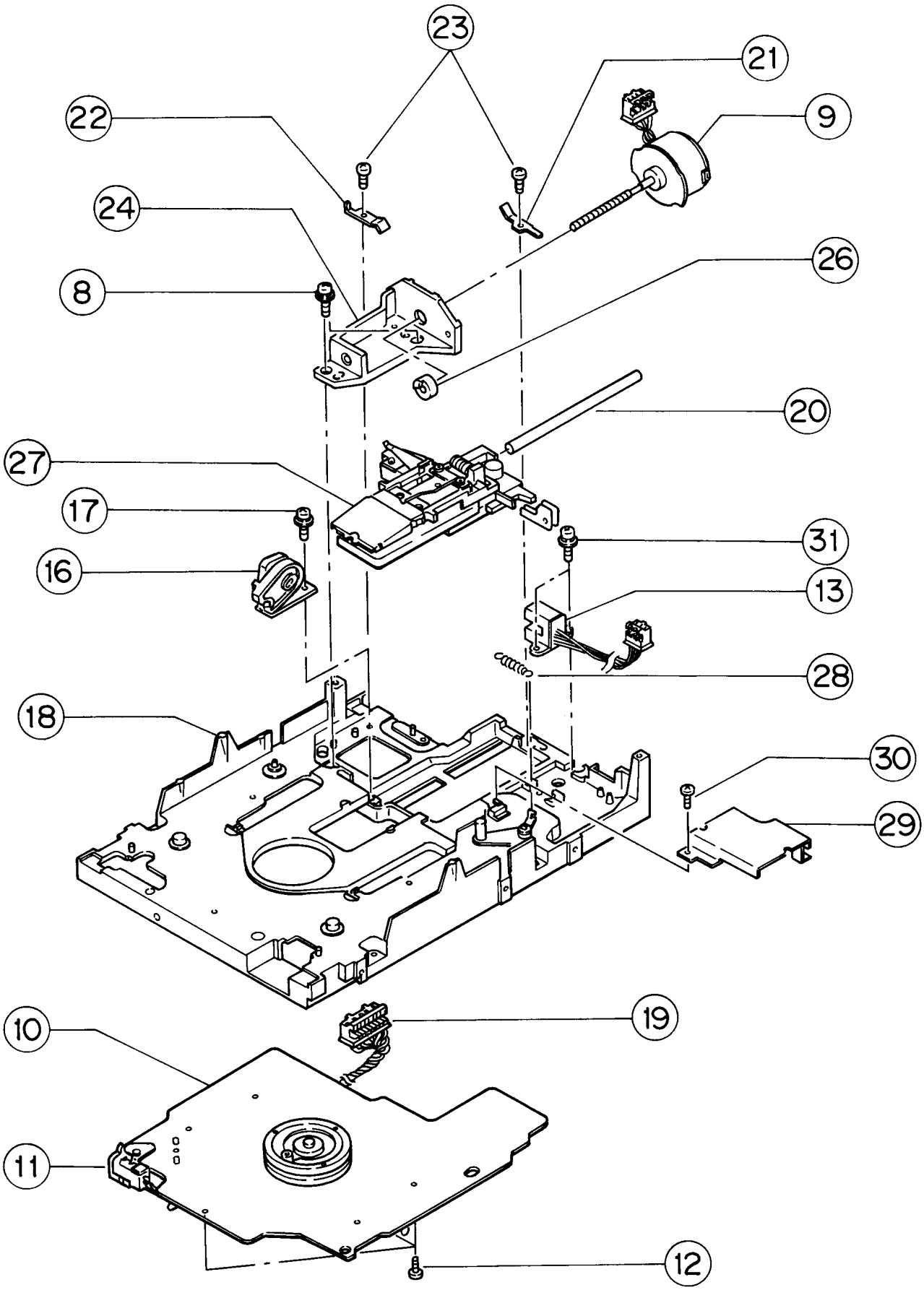
LU-7 BACK VIEW

LCD Unit Parts Location - B

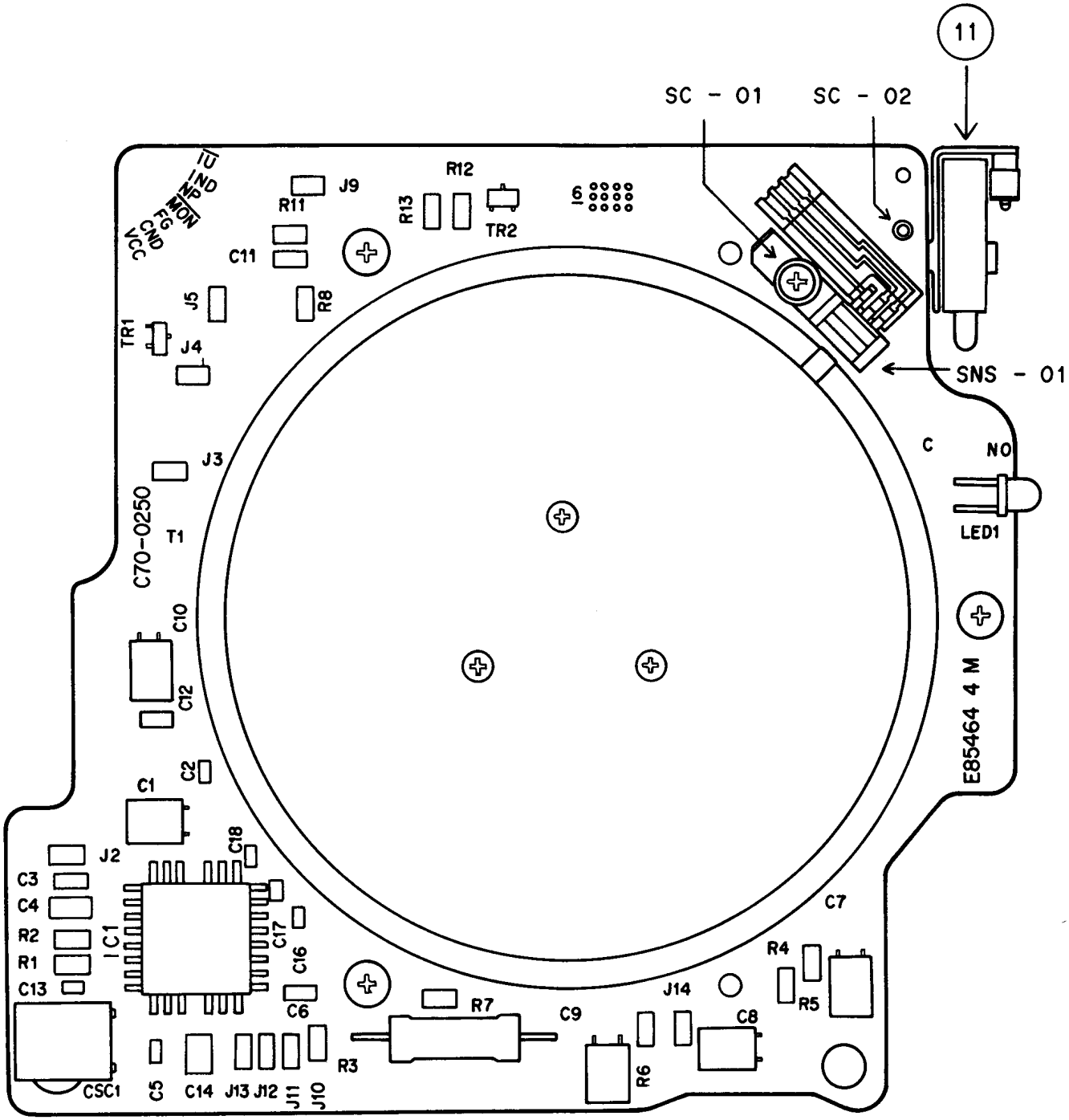


FDD Disassembly, Assembly and Parts

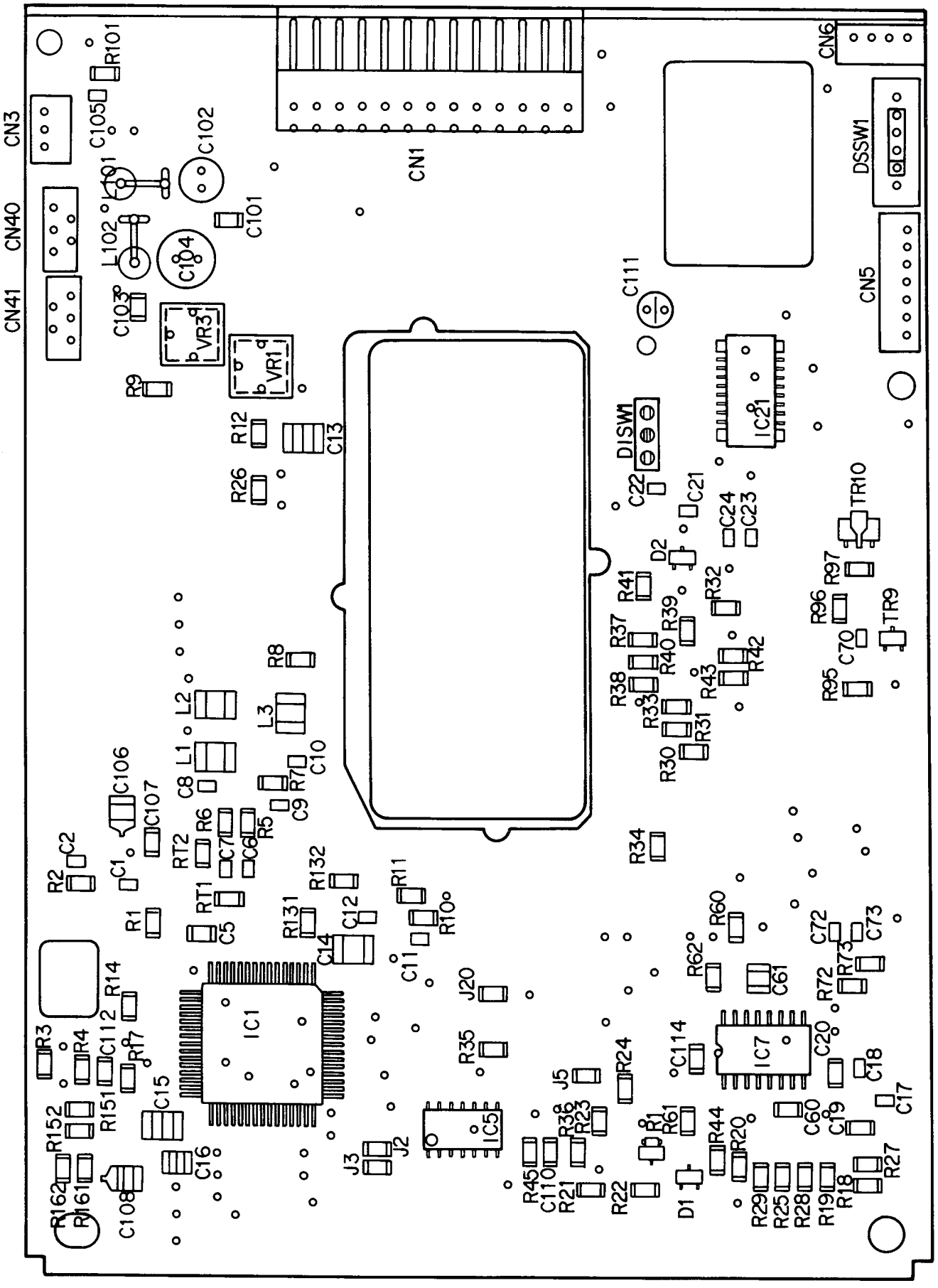




FDD Motor Spindle Parts Location



FDD PCB Control Parts Location



VI-2 Parts List

Main PCB Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
PCB.MAIN	P.C.B Assembly, Main (PCB.MAIN)		G1150-0130
BATTERY			
BATT1	3-FT-A, BATTERY (3.6V,50mA)		20214 – 032
BEADS and ferrite board			
BZ1	2943-666671, Ferrite,Six Hole		20200 – 314
BZ2 – 5	2643-000101, Ferrite Bead		20200 – 319
BF	MH30PA-12.7 × 10.2 × 1.0, Ferrite board		20000 – 028
CAPACITORS			
C1	Electrolytic, 33μF, 25V, ± 20%		20308 – 330
C2 – 3	Ceramic, 20PF, 50V, ± 5%		20308 – 321
C4 – 6	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C7 – 10	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C11 – 14	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C15 – 19	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C20	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C21 – 22	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C23	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C24 – 31	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C32	Ceramic, Trimmer, 20pF, +50%, −0%		20308 – 356
C33	Ceramic, 10pF, 50V, ± 0.5pF		20308 – 318
C34	Electrolytic, 10μF, 16V, ± 20%		20308 – 340
C35 – 36	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C37	Electrolytic, 10μF, 16V, ± 20%		20308 – 340
C38 – 39	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C40 – 41	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C42	Ceramic, 560pF, 50V, ± 10%		20308 – 315
C43	Ceramic, 10pF, 50V, ± 0.5pF		20308 – 317
C44	Not used		
C45	Ceramic, 10pF, 50V, ± 0.5pF		20308 – 317
C46	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C47	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C48 – 49	Ceramic, 22pF, 50V, ± 10%		20308 – 322
C50	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C51	Ceramic, Trimmer , 30pF, +50%, −0%		20308 – 357
C52	Ceramic, 39pF, 50V, ± 10%		20308 – 316
C53	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C54	Electrolytic, 10μF, 16V, ± 20%		20308 – 340
C55 – 56	Electrolytic, 10μF, 25V, ± 20%		20308 – 343
C57	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C58	Electrolytic, 10μF, 25V, ± 20%		20308 – 343
C59	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C60	Electrolytic, 100μF, 25V, ± 20%		20308 – 333
C61	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C62	Electrolytic, 100μF, 16V, ± 20%		20308 – 342
C63	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
C64	Electrolytic, 1μF, 50V, ± 20%		20308 – 332
C65	Ceramic, 0.047μF, 25V, +80%, −20%		20308 – 354
C66	Electrolytic, 100μF, 25V, ± 20%		20308 – 333
C67	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C68	Electrolytic, 1μF, 50V, ± 20%		20308 – 344
C69 – 71	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C72 – 73	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C74	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C75	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C76 – 77	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C78	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C79	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C80 – 81	Ceramic, 6pF, 50V, ± 5%		20308 – 323
C82 – 85	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C86 – 87	Ceramic, 47pF, 50V, ± 10%		20308 – 324
C88 – 90	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C91 – 92	Ceramic, 10pF, 50V, ± 0.5pF		20308 – 318
C93 – 94	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C95	Film, 0.1μF, 50V, ± 5%		20308 – 334
C96	Film, 3300pF, 50V, ± 5%		20308 – 335
C97	Film, 0.022μF, 50V, ± 5%		20308 – 365
C98	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C99 – 100	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C101	Ceramic, 0.1μF, 12V, +80%, −20%		20308 – 352
C102	Ceramic, 0.01μF, 16V, ± 20%		20308 – 320
C103 – 113	Ceramic, 220pF, 50V, ± 10%		20308 – 319
C114	Ceramic, 2.2μF, 25V, +80%, −20%		20308 – 351
CG1 – 5	Ceramic, 0.1μF,12V, +80%, −20%		20308 – 352
CONNECTORS			
CN1	Female,IRGB DB – 9 Pin		20204 – 1078
CN2	Female,LCD , 20 Pin		20204 – 1080
CN3	Pin JACK, VIDEO COMPOSITE		20000 – 027
CN4	Male, POWER PCB, 8 Pin		20204 – 1082
CN5	Male, SPEAKER, 2 Pin		20204 – 1084
CN6	Not used		
CN7A ,CN7B	Female,INTERNAL KEYBOARD, 10 Pin		20204 – 1086
CN8	Female,EXTERNAL KEYBOARD DIN5, 5 Pin		20204 – 1087
CN9	Female,PRINTER DB – 25 Pin		20204 – 1088
CN10	Female,INTERNAL FDD , 26 Pin		20204 – 1089
CN11	Female, EXT FDD DB – 37 Pin		20204 – 1091
CN12	Female, EXP BOX, 60 Pin		20204 – 1093
CN13	Male, RS-232C DB – 9 Pin		20204 – 1094
CN14	Female, EXP RAM , 26 Pin		20204 – 1089
CN15	Female, MODEM , 20 Pin		20204 – 1098
CN16	Male, LED , 6 Pin		20204 – 1100
CN17	Male, EL , 2 Pin		20204 – 1102

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
CRYSTALS			
CTL1	CSA309 – 14.318 MHz, Main Clock		20312 – 023
CTL2	CSA309 – 21.4772MHz, CRT Clock		20312 – 024
CTL3	HC-43U – 1.8432 MHz, COM1 Clock		20312 – 029
CTL4	S-308 – 32.768 KHz, RTC Clock		20312 – 026
CTL5	CSA309 – 6.000 MHz, SUB CPU Clock		20312 – 027
CLT6	CSA309 – 16.00 MHz, VFO Clock		20312 – 028
DIODES			
D1 – 8	1S2473, Silicon		20315 – 136
D9	Not used		
D10	1S2473, Silicon		20315 – 136
DIP SWITCH			
DP1	Switch DIP Type 2bit		20207 – 678
ICS and Gate Arrays			
IC1	V20, D70108C-8 8MHz		20301 – 423
IC2	MB675149U , Custom Gate Array Clock Generator, C-MOS		20301 – 424
IC3	D71088C Bus Controller, C-MOS		20301 – 425
IC4 – 6	M74HC373P, Octal Latch, C-MOS		20301 – 446
IC7	M74HC245P, Octal Bus Transceiver, C-MOS		20301 – 447
IC8	D71059C Interrupt Controller, C-MOS		20301 – 426
IC9	8087, Co – Processor (Option Part)		
IC10 – 11	MC74HC125, Quad Noninverting buffers, C-MOS		20301 – 448
IC12 – 14	D74HC244C, Octal buffer, C-MOS		20301 – 449
IC15	MB83128,128K Bit BIOS ROM C-MOS, U.S.A.		20301 – 450
IC16	MC74HC125, Quad Noninverting buffers, C-MOS		20301 – 448
IC17	M74HC245P, Octal Bus Transceiver, C-MOS		20301 – 447
IC18	TMP82C37AP-5, DMA Controller, C-MOS		20301 – 428
IC19	M74HC373P, Octal Latch, C-MOS		20301 – 446
IC20	D74HC244C, Octal buffer, C-MOS		20301 – 449
IC21	D71054C, Timer/Counter, C-MOS		20301 – 429
IC22	M74HC245P, Octal Bus Transceiver, C-MOS		20301 – 447
IC23 – 24	D74HC244C, Octal buffer, C-MOS		20301 – 449
IC25	M74HC374P, Octal Noninverting D-type Flip-Flop, C-MOS		20301 – 451
IC26	MB83128, 128K Bit Character Generator, ROM, C-MOS, U.S.A.		20301 – 490
IC27	M74HC166P,8-Bit serial or Parallel-Input/Serial-Output,C-MOS		20301 – 453
IC28 – 29	MB8464A-10L-SK, D4364CX-12L, 8K BYTE SRAM (Video RAM), C-MOS		20301 – 454
IC30	V6355D-F, LCD Controller, C-MOS		20301 – 430
IC31	M74ALS244AP, Octal buffer, TTL		20301 – 455
IC32	SN74HC240N, Octal Inverting buffer,C-MOS		20301 – 456
IC33	D74HC244C, Octal buffer, C-MOS		20301 – 449
IC34	BA4558, Bias AMP, Linear IC		20301 – 431

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
IC35	TC8570P, NS16C450N Programmable Communication Interface, C-MOS		20301 – 432
IC36	RP5C15, Real Time Clock, C-MOS		20301 – 433
IC37	SN74HC243N, Quad Bus Transceiver, C-MOS		20301 – 457
IC38	2903D Comparator, Linear IC		20301 – 434
IC39	LM386, Speaker AMP, Linear IC		20301 – 435
IC40 – 41	TC74HC157P, Quad 2-Input Data Selectors/Multiplexers, C-MOS		20301 – 458
IC42	M74HC245P, Octal Bus Transceiver, C-MOS		20301 – 447
IC43 – 44	MB81C4256-12P,M5M44C256-12, TC514256P10, 256 × 4 BIT DRAM,C-MOS		20301 – 459
IC45	EDL – 60, Active Delay Line		20301 – 436
IC46	TC74HC157P, Quad 2-Input Data Selectors/Multiplexers, C-MOS		20301 – 458
IC47	DS14C88N, RS-232C Driver, C-MOS		20301 – 460
IC48 – 49	DS14C89AN, RS-232C Receiver, C-MOS		20301 – 488
IC50	M80C49-770, Keyboard CPU, C-MOS		20301 – 437
IC51	MM74HC42N, MC74HC42N, 1-of-10 Decoder, C-MOS		20301 – 461
IC52	MC74HC03, Nand Gate With Open-Drain output, C-MOS		20301 – 462
IC53	74LS125A, Noninverting buffer, TTL		20301 – 463
IC54	D72065C, Floppy Disk Controller, C-MOS		20301 – 438
IC55	M74ALS240AP, Octal Inverting buffer, TTL		20301 – 464
IC56	M74HC04P, HEX Inverter, C-MOS		20301 – 465
IC57	SED9420CAC, VFO, C-MOS		20301 – 439
IC58	MC74HC14, HEX Schmitt-Trigger Inverter, C-MOS		20301 – 381
IC59	MC74HC365, HEX 3-State buffers With Common Enable, C-MOS		20301 – 466
GATE1	M60011-0117SP, Custom Gate Array,C-MOS		20301 – 440
GATE2	M60011-0118SP, Custom Gate Array,C-MOS		20301 – 441
GATE3	M60011-0115SP, Custom Gate Array,C-MOS		20301 – 442
GATE4	M60012-0116SP, Custom Gate Array,C-MOS		20301 – 443
GATE5	M60011-0116SP, Custom Gate Array,C-MOS		20301 – 444
IC sockets			
ICS1	IC Socket 40Pin		20209 – 186
ICS2 – 3	IC Socket 20Pin		20209 – 189
ICS4	IC Socket 28Pin		20209 – 188
ICS5 – 8	Not used		
ICS9	IC Socket 40Pin		20209 – 186
COIL INDUCTORS			
L1	SP0406-R68M-6, 0.68μH, 550mA		20307 – 016
L2	SP0406-180K, 18μH, 410mA		20307 – 017
L3	SP0408-R15M, 0.15μH, 1980mA		20307 – 018

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
RESISTORS:	*Unless otherwise specified resistors are 1/5W,* ± 5%, carbon type.		
R1	30K ohm		20316 – 453
R2	10K ohm		20316 – 438
R3 – 4	4.7K ohm		20316 – 458
R5 – 7	47K ohm		20316 – 459
R8	4.7K ohm		20316 – 458
R9	5.6K ohm		20316 – 463
R10	100K ohm		20316 – 439
R11 – 12	220 ohm		20316 – 634
R13	2.7K ohm		20316 – 449
R14	Carbon, 75 ohm, 1/4W, ± 5%		20316 – 635
R15 – 16	100K ohm		20316 – 439
R17	10 ohm		20316 – 435
R18	POTENTIOMETER 100K ohm 1/20W		20316 – 489
R19	30K ohm		20316 – 453
R20	8.2K ohm		20316 – 468
R21 – 22	4.7K ohm		20316 – 458
R23	1M ohm		20316 – 440
R24	1.5K ohm		20316 – 441
R25	2.7K ohm		20316 – 449
R26	1K ohm		20316 – 437
R27	10K ohm		20316 – 438
R28	1K ohm		20316 – 437
R29	6.8K ohm		20316 – 465
R30	2.7K ohm		20316 – 449
R31	47K ohm		20316 – 459
R32	560K ohm		20316 – 464
R33	Metal, 10K ohm, 1/5W, ± 1%		20316 – 478
R34	4.7 ohm		20316 – 460
R35	4.7K ohm		20316 – 458
R36	10K ohm		20316 – 438
R37	Metal, 10K ohm, 1/5W, ± 1%		20316 – 478
R38	2.7K ohm		20316 – 449
R39	270K ohm		20316 – 451
R40	Metal, 11.3K ohm, 1/5W, ± 1%		20316 – 636
R41	4.7K ohm		20316 – 458
R42	10K ohm		20316 – 438
R43	Metal, 10K ohm, 1/5W, ± 1%		20316 – 478
R44	2.7K ohm		20316 – 449
R45	270K ohm		20316 – 451
R46	100K ohm		20316 – 439
R47	POTENTIOMETER 100K ohm, 1/10W, ± 30%		20316 – 488
R48	10K ohm		20316 – 438
R49 – 50	1K ohm		20316 – 437
R51	Carbon, 1.5K ohm, 1/4W, ± 5%		20316 – 474
R52 – 53	100K ohm		20316 – 439
R54	Carbon, 330 ohm, 1/4W, ± 5%		20316 – 475
R55	27K ohm		20316 – 450
R56	1.6K ohm		20316 – 442
R57	16K ohm		20316 – 443
R58 – 60	22 ohm		20316 – 445
R61	100K ohm		20316 – 439

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
R62 – 64	820 ohm		20316 – 466
R65	47K ohm		20316 – 459
R66	4.7K ohm		20316 – 458
R67	47K ohm		20316 – 459
R68 – 69	4.7K ohm		20316 – 458
R70	1M ohm		20316 – 440
R71	Metal, 100 ohm, 1/5W, ± 1%		20316 – 477
R72	Metal, 33K ohm, 1/5W, ± 1%		20316 – 482
R73	Metal, 7.5K ohm, 1/5W, ± 1%		20316 – 483
R74	Metal, 2.4K ohm, 1/5W, ± 1%		20316 – 481
R75	100K ohm		20316 – 439
R76 – 77	See LED PCB		
R78	1M ohm		20316 – 440
R79	2.2K ohm		20316 – 446
R80	1K ohm		20316 – 437
R81 – 83	100K ohm		20316 – 439
RESISTOR NETWORKS: *resistor networks are 1/8W, ± 5%.*			
RA1	47K ohm × 5		20316 – 425
RA2	47K ohm × 4		20316 – 426
RA3 – 5	47K ohm × 8		20316 – 428
RA6	Not used		
RA7	47K ohm × 8		20316 – 428
RA8	100K ohm × 4		20316 – 427
RA9	100K ohm × 3		20316 – 431
RA10	47K ohm × 4		20316 – 426
RA11	47K ohm × 8		20316 – 428
RA12	47K ohm × 4		20316 – 426
RA13	47K ohm × 3		20316 – 434
RA14	47K ohm × 8		20316 – 428
RA15	10K ohm × 9		20316 – 429
RA16	10K ohm × 5		20316 – 430
RA17	10K ohm × 3		20316 – 432
RA18	10K ohm × 5		20316 – 430
RA19	47K ohm × 8		20316 – 428
RA20	4.7K ohm × 5		20316 – 433
SWITCHES			
SW1	Not used		
SW2	Switch Slide(1-2) MONITOR ON/OFF		20207 – 675
SW3	Switch Slide(2-4) BOOT SELECT		20207 – 676
TRANSISTORS			
TR1	DTC114ES, NPN Type (Degitra)		20317 – 134
TR2	DTA114ES, PNP Type (Degitra)		20317 – 135
TR3	2SC1741DZR, NPN Type		20317 – 138
TR4 – 5	JA101, PNP Type		20317 – 139
TR6	JC501, NPN Type		20317 – 149
TR7	DTC114TS, NPN Type (Degitra)		20317 – 136
TR8	Not used		
TR9	DTC114TS, NPN Type (Degitra)		20317 – 136

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
TR10	DTC114ES, NPN Type (Degitra)		20317 – 134
TR11	DTA114ES, PNP Type (Degitra)		20317 – 135
TR12	DTB114ES, PNP Type (Degitra)		20317 – 137
TR13	DTC114ES, NPN Type (Degitra)		20317 – 134
TR14	2SA934DZR, PNP Type		20317 – 141
TR15 – 16	DTC114ES, NPN Type (Degitra)		20317 – 134
TR17	2SB1182R, PNP Type		20317 – 142
TR18 – 38	DTC114ES, NPN Type (Degitra)		20317 – 134
ZENER DIODE			
ZD1	02BZ4.7A, Zener		20315 – 163
CONNECTOR ASSIES			
CN1 – ASSY	Not used		
CN2 – ASSY	LCD (ASSY), 20 Pin		20204 – 1079
CN3 – ASSY	Not used		
CN4 – ASSY	See Power PCB Assembly		
CN5 – ASSY	SPEAKER (ASSY), 2 Pin		20204 – 1085
CN (6-9) – ASSY	Not used		
CN10 – ASSY	INTERNAL FDD (ASSY), 2 Pin		20204 – 1090
CN11 – ASSY	Not used		
CN12 – ASSY	EXP BOX (ASSY), 60 Pin		20204 – 1092
CN13 – ASSY	Not used		
CN14 – ASSY	EXP RAM (ASSY), 26 Pin		20204 – 1095
CN15 – ASSY	MODEM (ASSY), 20 Pin		20204 – 1097
CN16 – ASSY	LED (ASSY), 6 Pin		20204 – 1099
CN17 – ASSY	See Power PCB Assembly		
CNBATT – ASSY	See Power PCB Assembly		

Power PCB Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
PCB.POWER	P.C.B Assembly, POWER(PCB.POWER)		G1150-0138
CAPACITORS			
C500	Electrolytic, 220μF, 25V, ± 20%		20308 – 327
C501	Ceramic, 470pF, 50V, ± 10%		20308 – 358
C502	Film, 2200pF, 50V, ± 10%		20308 – 325
C503	Film, 0.01μF, 50V, ± 10%		20308 – 326
C504 – 505	Electrolytic, 100μF, 25V, ± 20%		20308 – 333
C506	Electrolytic, 47μF, 25V, ± 20%		20308 – 328
C507 – 509	Electrolytic, 22μF, 25V, ± 20%		20308 – 329
C510	Electrolytic, 1μF, 50V, ± 20%		20308 – 341
C511	Ceramic, 0.01μF, 50V, +80%, −20%		20308 – 349
C512 – 513	Film, 0.01μF, 50V, ± 10%		20308 – 326
C514	Film, 0.001μF, 50V, ± 5%		20308 – 338
C515	Film, 2200pF, 50V, ± 10%		20308 – 325
C516	Electrolytic, 470μF, 25V, ± 20%		20308 – 331
C517	Film, 470pF, 50V, ± 5%		20308 – 339
C518	Film, 0.01μF, 50V, ± 10%		20308 – 326
C519	Ceramic, 470pF, 50V, ± 10%		20308 – 358
C520 – 522	Electrolytic, 330μF, 16V, ± 20%		20308 – 345
C523	Ceramic, 1μF, 50V, +80%, −20%		20308 – 350
C524	Electrolytic, 10μF, 25V, ± 20%		20308 – 343
C525	Film, 0.047μF, 50V, ± 10%		20308 – 337
C526 – 527	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C528 – 529	Ceramic, 0.01μF, 50V, ± 20%		20308 – 355
C530	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C531	Electrolytic, 1μF, 50V, ± 20%		20308 – 346
C532	Ceramic, 0.1μF, 25V, +80%, −20%		20308 – 353
C533	Electrolytic, 2200μF, 25V, ± 20%		20308 – 347
CONNECTOR ASSIES			
CN4 – ASSY	POWER PCB (ASSY), 8 Pin		20204 – 1083
CN17 – ASSY	EL (ASSY), 2 Pin		20204 – 1101
CNBATT – ASSY	BATTERY (ASSY), 2 Pin		20204 – 1108
DIODES			
D500	1SS133, High Speed Switching		20315 – 156
D501 – 503	1SS136, VH Speed Switching		20315 – 157
D504	1SS130, High Speed Switching		20315 – 158
D505	ERC81-004, Schottky Barrier		20315 – 159
D506	GP-20B, Silicon		20315 – 160
D507	EK04, Schottky Barrier		20315 – 173
D508 – 509	SB3400 Schottky Barrier		20315 – 162
FUSE			
F500	FUSE 2A		20217 – 124
JACK			
JACK1	JACK AC		20000 – 025
HEAT SINK			
HS500	Cooler For TR511		20300 – 051
HS501	Cooler For TR512		20300 – 052

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
IC			
IC500	μPC494C, Regulator Controller, Bipolar IC		20301 – 445
COIL INDUCTORS			
L500	CKL-02, 15μH		20307 – 021
L501 – 503	SP0406-220K-6, 22μH		20307 – 020
L504	CKL-01, 110μH		20307 – 022
L505 – 506	SP0408-1R5K, 1.5μH		20307 – 019
TEST POLE			
POLE1 – 4	Test Point Check Pole		20000 – 026
RESISTORS: *Unless otherwise specified, resistors are 1/5W, ± 5%, Carbon type.*			
R500	2.2K ohm		20316 – 446
R501	30K ohm		20316 – 453
R502 – 503	10K ohm		20316 – 438
R504	Carbon, 3.3K ohm, 1/4W, ± 5%		20316 – 471
R505	56 ohm		20316 – 461
R506 – 507	100K ohm		20316 – 439
R508	4.7K ohm		20316 – 458
R509	560K ohm		20316 – 464
R510	100K ohm		20316 – 439
R511	220K ohm		20316 – 448
R512	22K ohm		20316 – 447
R513	27K ohm		20316 – 450
R514	10K ohm		20316 – 438
R515	Metal, 1.82 (1.87,1.91,1.96,2) K ohm, 1/5W, ± 1%		20316 – 491
R516	Metal, 4.7K ohm, 1/5W, ± 1%		20316 – 484
R517	2.7K ohm		20316 – 449
R518	3.9K ohm		20316 – 456
R519	330K ohm		20316 – 455
R520	33 ohm		20316 – 454
R521	Carbon, 47 ohm, 1/4W, ± 5%		20316 – 472
R522	16K ohm		20316 – 443
R523	270K ohm		20316 – 451
R524	Metal, 5.6K ohm 1/5W, ± 1%		20316 – 485
R525	10K ohm		20316 – 438
R526	Metal, 5.6K ohm 1/5W, ± 1%		20316 – 485
R527	6.8K ohm		20316 – 465
R528	27K ohm		20316 – 450
R529	270K ohm		20316 – 451
R530 – 531	470 ohm		20316 – 457
R532	22K ohm		20316 – 447
R533	1K ohm		20316 – 437
R534	22K ohm		20316 – 447
R535	4.7K ohm		30316 – 458
R536	560 ohm		20316 – 462
R537	2.2K ohm		20316 – 446
R538 – 539	1K ohm		20316 – 437
R540	470 ohm		20316 – 457

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
R541	10K ohm		20316 – 438
R542	5.6K ohm		20316 – 463
R543	Carbon, 220 ohm, 1/4W, ± 5%		20316 – 637
R544	Carbon, 270 ohm, 1/4W, ± 5%		20316 – 470
R545	22 ohm		20316 – 445
R546	Curled wire, 0.05 ohm, ± 5%		20316 – 487
R547	Carbon, 68 ohm, 1/4W, ± 5%		20316 – 473
R548	Carbon, 22 ohm, 1/4W, ± 5%		20316 – 490
R549	Metal, 4.99 (5.11,5.23,5.36,5.49, 5.6,5.62,5.76) K ohm, 1/4(1/5)W, ± 1%		20316 – 641
R550	Metal, 5.6K ohm 1/5W, ± 1%		20316 – 485
R551	Carbon, 100 ohm, 1/5W, ± 5%		20316 – 436
R552	6.8K ohm		20316 – 465
R553	33 ohm		20316 – 454
R554	DX Metal, 27 ohm 2W, ± 2%		20316 – 486
THYRISTOR			
SCR500	5P4M, Thyristor		20309 – 004
SWITCH			
SW500	Switch, Rocker, Power Supply, Black		20207 – 671
TRANSFORMERS			
T500	CKT-01,Transformer DC/DC Convertor		20215 – 033
T501	CKT-02,Transformer EL Invertor		20215 – 034
T502	SC-02-06G,Transformer Troidal Core		20215 – 035
TRANSISTORS			
TR500	2SA1315Y, PNP Type		20317 – 143
TR501 – 505	JC501, NPN Type		20317 – 149
TR506 – 507	JA101, PNP Type		20317 – 139
TR508	2SC3303, NPN Type		20317 – 144
TR509	2SC2001-F, NPN Type		20317 – 145
TR510	2SA950-Y, PNP Type		20317 – 146
TR511	2SA1328Y, PNP Type		20317 – 147
TR512	2SC2516K, NPN Type		20317 – 148
ZENER DIODES			
ZD500	MTZ 4.7A, Zener 4.7V		20315 – 164
ZD501	RD 5.1FB3 , Zener 5.1V		20315 – 165
ZD502	MTZ16C, Zener 16V		20315 – 166

SUB PCB Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
PCB.SUB	P.C.B Assembly, SUB(PCB.SUB)		G1150 – 0183
CAPACITORS			
C534	Ceramic, 0.33μF, 50V, +80%, −20%		20308 – 368
C535	Film, 1000pF, 50V, ± 10%		20308 – 366
C536	Electrolytic, 47μF, 25V, ± 20%		20308 – 367
DIODES			
D510	EK04, Schottky Barrier		20315 – 173
D511	1SR139, Silicon		20315 – 161
IC			
IC501	M5237L, Regulator Controller, Bipolar IC		20301 – 501
RESISTORS: *Unless otherwise specified, resistors are 1/5W,* ± 5%, Carbon type.			
R555	47K ohm		20316 – 640
R556	Metal, 4.87K ohm, 1/5W, ± 1%		20316 – 639
R557	220 ohm		20316 – 638
TRANSISTOR			
TR513	2SB1182P-CPT, PNP Type		20317 – 152
WIRE LEAD			
WIRE-RED	UL1007AWG24L, 70mm, RED		20213 – 298
WIRE-BLUE	UL1007AWG24L, 70mm, BLUE		20213 – 299
WIRE-BLACK	UL1007AWG24L, 70mm, BLACK		20213 – 300
WIRE-YELLOW	UL1007AWG24L, 70mm, YELLOW		20213 – 301

MEMORY PCB Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
PCB.MEMORY	P.C.B Assembly, MEMORY (PCB.MEMORY)		G1150 – 0137
CAPACITORS			
C300 – 303	Ceramic 0.1μF, 12V, +80%, −20%		20308 – 352
C304 – 305	Electrolytic, 22μF, 16V, ± 20%		20308 – 348
C306 – 308	Ceramic 0.01μF, 16V, ± 20%		20308 – 320
ICS			
IC300 – 303	MB81C4256-12P, M5M44C256-12, TC514256P10,256 × 4 bit DRAM,C-MOS		20301 – 459
IC304	TC74HC08P, M74HC08P, MN74HC08, 2 Input And Gate, C-MOS		20301 – 489
IC305	M74HC04P, HEX Inverter, C-MOS		20301 – 465
IC306	EDL-040, Active Delay Line		20301 – 487
IC SOCKETS			
ICS300 – 303	20 Pin IC Socket		20209 – 187
RESISTORS			
R300 – 302	Carbon, 22 ohm, 1/4W, ± 5%		20316 – 469

LED PCB Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
PCB.LED	P.C.B Assembly, LED (PCB.LED)		H115- – 0146
LEDS			
LED1	SLB25MG, LED GREEN		20315 – 167
LED2 – 5	SLB25VR, LED RED		20315 – 168
RESISTORS			
R76 – 77	Carbon, 820 ohm 1/4W, ± 5%		20316-467
SPEAKER			
SP1	DMS-2845-CZ, Speaker		20332 – 001
BATTERY			
BATT2	10KR-2000C, 12V, 2200mAH, BATTERY MAIN		20214 – 031
AC ADAPTER			
AC ADAPTER	ADAPTER AC120-DC15V (UL)		20200 – 318
SYSTEM FLOPPY DISK			
SYSTEM DISK	SYSTEM FLOPPY DISK (USA)		40132 – 025

LCD UNIT Assembly

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
LCD	DISPLAY LCD Assembly		20341 – 001
LU-0	MODULE, CELL, & PCB		L31 – 0010
LU-1	HOLDER, CELL		L12 – 0360
LU-2	RUBBER SEAT		L15 – 0260
LU-3	CELL, LCD		L01 – 3450
LU-4	RUBBER CONNECTOR		L14 – 0351
LU-5	EL, BACK LIGHT		L16 – 0220
LU-6	HEAT SEAL		L13 – 0190
LU-7	ASSY, PCB.LCD		L30 – 0570
CAPACITOR			
LU-7-7	Electrolytic, 4.7μF, 35V, $\pm$ 20%		L23 – 0080
ICS			
LU-7-1	M5298, Common Driver		L20 – 0240
LU-7-2	M5299B, Segment Driver		L20 – 0250
LU-7-3	HC4040, 12-Stage Binary Counter		L20 – 0400
LU-7-8	μPC324G, 2902 OP-AMP		L25 – 0010
RESISTORS			
LU-7-4	Chip(Metal), 7.5K ohm, 1/8W, $\pm$ 1%		L22 – 0361
LU-7-5	Chip(Metal), 39K ohm, 1/8W, $\pm$ 2%		L22 – 0471
LU-7-6	Chip(Metal), 100 ohm, 1/8W, $\pm$ 2%		L22 – 0391
TRANSISTOR			
LU-7-9	2SA1235, PNP Type		897 – 0180T
WIRES			
LU-8	Wire, EL, White		L26 - 0310
LU-9	Wire, EL, Black		L26 – 0300
CONNECTORS			
CN2 – L.UNIT	LCD (LCD Unit), 20 Pin		20204 – 1081

FDD

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
FDD	Floppy Disk Drive		70433 – 001
1	Screw,PCB,Control,Pan Head,M2.5 × 4		Y13 – 8402
2	Assy, PCB, Control (Prefix F is omitted on the reference drawing)		C60 – 0390
CAPACITORS			
FC1 – 2	Ceramic, 33pF, 50V, ± 5%		W52 – 3301
FC3 – 4	Not used		
FC5	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
FC6 – 7	Ceramic, 0.01μF, 50V, ± 10%		W32 – 1032
FC8	Ceramic, 680pF, 50V, ± 5%		W52 – 6811
FC9	Ceramic, 47pF, 50V, ± 5%		W52 – 4701
FC10	Ceramic, 0.001μF, 50V, ± 10%		W32 – 1022
FC11 – 12	Ceramic, 330pF, 50V, ± 5%		W52 – 3311
FC13	Ceramic, 0.01μF, 25V, ± 5%		W57 – 1036
FC14	Ceramic, 0.01μF, 50V, ± 5%		W67 – 1031
FC15	Ceramic, 0.01μF, 25V, ± 5%		W57 – 1036
FC16	Ceramic, 0.15μF, 25V, ± 10%		W34 – 1547
FC17	Ceramic, 0.01μF, 50V, ± 10%		W32 – 1032
FC18	Ceramic, 100pF, 50V, ± 10%		W52 – 1012
FC19	Tantalum, 1μF, 16V, ± 10%		C77 – 0230
FC20	Tantalum, 1μF, 16V, ± 20%		C77 – 0050
FC21 – 24	Ceramic, 100pF, 50V, ± 10%		W52 – 1012
FC25 – 59	Not used		
FC60	Tantalum, 1μF, 16V, ± 10%		C77 – 0230
FC61	Ceramic, 0.15μF, 25V, ± 10%		W34 – 1547
FC62 – 69	Not used		
FC70	Ceramic, 4200pF, 50V, ± 10%		W32 – 4722
FC71	Not used		
FC72 – 73	Ceramic, 0.01μF, 50V, ± 10%		W32 – 1032
FC74 – 100	Not used		
FC101	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
FC102	Electrolytic, Aluminium, 22μF, 16V, ± 20%		C77 – 0210
FC103	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
FC104	Electrolytic, Aluminium, 33μF, 16V, ± 20%		C77 – 0220
FC105	Ceramic, 0.01μF, 50V, ± 10%		W32 – 1032
FC106	Tantalum, 3.3μF, 20V, ± 20%		C77 – 0240
FC107	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
FC108	Tantalum, 3.3μF, 20V, ± 20%		C77 – 0240
FC109	Not used		
FC110	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
FC111	Electrolytic, Aluminium, 3.3μF, 50V, ± 20%		C77 – 0280
FC112	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
FC113	Not used		
FC114	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
COILS			
FL1 – 2	Inductor, 680μH		C79 – 0150
FL3	Inductor, 150μH		C79 – 0160
FL4 – 100	Not used		
FL101 – 102	Inductor, Ferrite Bead Type		C79 – 0090
FCH1	Cover, Head		C37 – 0330
CONNECTORS			
FCN1	FCN-725P026-AU/O-HN, 26Pin		C84 – 0090
FCN2	Not used		
FCN3	B-3-B-PH, 3Pin		C84 – 0120
FCN4	Not used		
FCN5	See REF.NO 19		
FCN6	B-4-B-PH, 4Pin		C84 – 0010
FCN7 – 39	Not used		
FCN40 – 41	IL-FPC-5S S1T1, 5Pin		C84 – 0130
DIODES			
FD1 – 2	Diode Array, Silicon DAP202 KT-96		C80 – 0210
VOLUMES			
FVR1	Pot, Semi-Fixed, 30K ohm Curve (B) Volume For Asymmetry Adjust And Erase Signal Timing		C76 – 0060
FVR2	Not used		
FVR3	Pot, Semi-Fixed, 30K ohm Curve (B) Volume For Asymmetry Adjust And Erase Signal Timing		C76 – 0060
ICS			
FIC1	M52811FP, Read/Write Control, Bi-CMOS		C71 – 0380
FIC2 – 4	Not used		
FIC5	BU74HC00F, Nand Gate, CMOS		C71 – 0070
FIC6	Not used		
FIC7	T74HC123, Monostable Multivibrator, CMOS		C71 – 0300
FIC8 – 20	Not used		
FIC21	LB1633, Stepping Motor Driver		C71 – 0420
JUMPER CHIP			
FJ1	Not used		
FJ2 – 3	Jumper Chip ERJ-8GCYO-ROOV 2A, $\leqq$ 50m OHM		W21 – 0R00
FJ4	Not used		
FJ5	Jumper Chip ERJ-8GCYO-ROOV 2A, $\leqq$ 50m OHM		W21 – 0R00
FJ6 – 19	Not used		
FJ20	Jumper Chip ERJ-8GCYO-ROOV 2A, $\leqq$ 50m OHM		W21 – 0R00

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
RESISTORS: Unless otherwise specified, resistors are 1/8W, ± 5%, Metal Type.			
FRT1 – 2	560 ohm		W21 – 5613
FR1 – 2	3.3K ohm		W21 – 3323
FR3 – 4	10K ohm		W21 – 1033
FR5 – 6	1K ohm, 1/8W, ± 2%, Metal		W21 – 1022
FR7	2.2K ohm		W21 – 2223
FR8	300 ohm		W21 – 3013
FR9	10K ohm		W21 – 1033
FR10	8.2K ohm, 1/8W, ± 2%, Metal		W21 – 8222
FR11	4.3K ohm		W21 – 4323
FR12	120K ohm		W21 – 1243
FR13	Not used		
FR14	5.6K ohm, 1/8W, ± 1%, Metal		W21 – 5621
FR15 – 16	Not used		
FR17	5.6K ohm, 1/8W, ± 1%, Metal		W21 – 5621
FR18 – 19	430K ohm		W21 – 4343
FR20	10K ohm		W21 – 1033
FR21	1.5K ohm		W21 – 1523
FR22	100K ohm		W21 – 1043
FR23	10K ohm		W21 – 1033
FR24	2.2K ohm		W21 – 2223
FR25	100K ohm		W21 – 1043
FR26	330 ohm		W21 – 3313
FR27	10K ohm		W21 – 1033
FR28 – 29	100K ohm		W21 – 1043
FR30 – 36	1K ohm		W21 – 1023
FR37 – 43	10K ohm		W21 – 1033
FR44	20 ohm		W21 – 2003
FR45	5.6K ohm		W21 – 5623
FR46 – 59	Not used		
FR60	5.6K ohm		W21 – 5623
FR61	750K ohm		W21 – 7543
FR62	430K ohm		W21 – 4343
FR63 – 71	Not used		
FR72 – 73	1K ohm		W21 – 1023
FR74 – 94	Not used		
FR95	5.6K ohm		W21 – 5623
FR96	180K ohm		W21 – 1813
FR97	10K ohm		W21 – 1033
FR98 – 100	Not used		
FR101	100K ohm		W21 – 1043
FR102 – 130	Not used		
FR131	2.7K ohm, 1/8W, ± 2%, Metal		W21 – 2722
FR132	39K ohm, 1/8W, ± 1%, Metal		W21 – 3931
FR133 – 150	Not used		
FR151	390K ohm, 1/8W, ± 1%, Metal		W21 – 3941
FR152	39K ohm, 1/8W, ± 1%, Metal		W21 – 3931
FR153 – 160	Not used		
FR161	270K ohm, 1/8W, ± 1%, Metal		W21 – 2741
FR162	12K ohm, 1/8W, ± 1%, Metal		W21 – 1231

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
TRANSISTOR			
FTR1	2SA1037KT-96, PNP Type		W11 – 1037
FTR2 – 8	Not used		
FTR9	2SC1621KT-B3/B4-T1, NPN Type		W13 – 1621
FTR10	2SB1120FTC, PNP Type		W12 – 1120
SWITCHES			
FDSSW1	NSL-10104-381, Driver Select		C85 – 0050
FDISW1	NSM-10102-276B, Cartridge In		C85 – 0060
3	Assy, Bezel, Front		C14 – 0130
3-1	Bezel, Front, Fawn-Grey		C50 – 0210
3-2	Shutter, Front, F – G		C52 – 0260
3-3	Spring, Shutter, Front		C36 – 0270
3-4	Cover, Lamp, RED		C28 – 0110
4	Button, Eject, Fawn –tGrey		C52 – 0300
5	Assy, Carrier (Non Repairable) Base, Carrier Shaft, Slide Roller Shaft, Lever, Shutter Switch Lever, Shutter Switch Base, Lever, Shutter Switch Pin, Lever, Shutter Switch Roller, Lever, Shutter Switch Spring, Lever, Shutter Switch Spring, Cartridge In		C10 – 0080
6	Spring, Plate, Slide		C36 – 0240
7	Plate, Slide		C23 – 0310
8	Screw, Motor, Stepping Pan Head With Spring Washer And Flat Washer, M2.0 × 5		C42 – 0160
9	Motor, Stepping		C06 – 0130
10	Assy Motor Spindle (Other Than Electrical parts Non Repairable. Prefix S is omitted on the reference drawing)		C04 – 0130
CAPACITORS			
SC1	Electrolytic, Aluminium, 100μF, 16V, ± 20%		C77 – 0260
SC2	Ceramic, 0.01μF, 50V, ± 10%		W32 – 1032
SC3	Ceramic, 0.047μF, 50V, ± 10%		W33 – 4732
SC4	Tantalum, 0.47μF, 16V, ± 20%		C77 – 0200
SC5	Ceramic, 47pF, 50V, ± 5%		W52 – 4701
SC6	Ceramic, 0.1μF, 25V, ± 20%		W33 – 1048
SC7 – 9	Electrolytic, Aluminium, 4.7μF, 25V, ± 20%		C77 – 0270
SC10	Electrolytic, Aluminium, 100μF, 16V, ± 20%		C77 – 0260
SC11 – 12	Ceramic, 0.1μF, 50V, +80%, −20%		W43 – 1044
SC13	Ceramic, 47pF, 50V, ± 5%		W52 – 4701
SC14	Ceramic, 0.47μF, 25V, +80%, −20%		W44 – 4749
SC15	Not used		
SC16 – 18	Ceramic, 0.01μF, 50V, ± 10%		W32 – 1032

REF.NO.	DESCRIPTION	RS PART NO.	MFR'S PART NO.
CONNECTOR			
FCN5(19)	Connector, B-7-B-PH, 7Pin		C84 – 0030
DIODE			
SLED1	Diode, Light Emitting, GL-3HD006 3.5mcd(Typ.) at if 20mA		C80 – 0200
IC			
SIC1	HA13440MP,Servo Control,Spindle Motor		C71 – 0430
RESISTORS: Unless otherwise specified, resistors are 1/8W, ± 5%, Metal Type.			
SR1	27K ohm		W21 – 2733
SR2	56K ohm		W21 – 5633
SR3	0.36 ohm, 1W, ± 5%		C75 – 0100
SR4 – 6	3.9 ohm		W21 – 3R93
SR7	270 ohm		W21 – 2713
SR8	220 ohm		W21 – 2213
SR9 – 10	Not used		
SR11 – 13	4.7K ohm		W21 – 4723
TRANSISTORS			
STR1	DTA143XK-T-96, PNP Type, Digital		C73 – 0130
STR2	DTC143XK-T-96, NPN Type, Digital		C73 – 0140
CRYSTAL			
SOSC1	Oscillator,Ceramic,CSB491E36,491.52KHz		C81 – 0060
JUMPER			
SJ1	Not used		
SJ2 – 5	Jumper Chip ,ERJ-8GCYO-ROOV, 2A, ≦50m ohm		W21 – 0R00
SJ6 – 8	Not used		
SJ9 – 14	Jumper Chip ,ERJ-8GCYO-R00V, 2A, ≦50m ohm		W21 – 0R00
SSNS-01	Assy Sensor Index		C66 – 0300
SSC-01	Screw, Sensor Index Pan Head With Spring Washer And Flat Washer M2.0 × 4		042 – 0220
SSC-02	Screw, Sensor Write Protect Pan Head With Spring Washer And Flat Washer M2.0 × 3		Y13 – 6305
11	Assy Sensor Writeprotect		C13 – 0030
12	Screw, Assy, Spindle Motor Pan Head, M2.5 × 2.8		Y41 – 8285
13	Sensor 00		C66 – 0270
14	Cover, Shield		C37 – 0390
15	Sheet, Insulation		C86 – 0250
16	Assy, Damper		C13 – 0010
17	Screw, Damper Pan Head With Spring Washer And Flat Washer, M2.0 × 6		C42 – 0080
18	Assy, Chassis (All Parts Rivetted, Non Repairable) Pin, Lock Roller, Pin, Lock		C00 – 0110
28	Spring, Lever, Lock		C36 – 0250
19	See REF.NO 10		
20	Shaft Guide		C31 – 0090
21	Holder, Shaft, Guide, Right		C25 – 0310

REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
22	Holder, Shaft, Guide, Left			C25 – 0320
23	Screw, Holder, Shaft, Guide Pan Head With Spring Washer And Flat Washer, M2.5 × 4			Y41 – 8402
24	Holder, Motor, Stepping			C20 – 0060
25	Not used			
26	Collar, Stopper, Carriage			C28 – 0240
27	Assy, Carriage (Non Repairable) Arm, Top, Complete Head, Top, Complete Carriage, Sub Assy Head, Bottom, Complete			C01 – 0120
28	See REF.NO 18			
29	Plate, Shield, Head, Terminal			C37 – 03401
30	Screw, Plate, Shield Head, Terminal Pan Head, M2.0 × 1.6			Y11 – 6165
31	Screw, Sensor 00,Pan Head With Spring Washer And Flat Washer, M2.0 × 5			C42 – 0160
Mechanical and Assembly Parts				
A1	Pedestral, Right	1		G100 – 0157
A2	Pedestral, Left	1		G100 – 0160
A3	Assy, Arm, Right, F – G	1		G100 – 0179
A4	Assy, Arm, Left, F – G	1		G100 – 0189
P1	Case, Bottom, Black	1		H100 – 0151
P2	Handle, Black	1		K100 – 0155
P3	Pin, Handle	2		K100 – 0156
P4	Insulator, PCB	1		K100 – 0163
P5	Shield Plate, Main PCB	1		K100 – 0164
P6	Rear Panel, Fawn – Grey	1		G100 – 0165
P7	Shield Plate, Keyboard	1		G100 – 0174
P8	Knob, Contrast, Black	1		K100 – 0167
P9	Base Frame	1		K100 – 0168
P10	Shield Plate FDD	1		K100 – 0169
P11	Box, Power Source PCB	1		K100 – 0170
P12	Pillar, Power Source PCB	4		K100 – 0171
P13	Cover, Power Source PCB	1		K100 – 0172
P14	Collar, Base Frame	2		K100 – 0173
P15	Washer, Keyboard	4		K100 – 0223
P16	Bracket, LED PCB	1		K100 – 0175
P17	Case, LCD, Fawn – Grey	1		H100 – 0177
P18	Cover, Lever, Right, F – G	1		H100 – 0206
P19	Cover, Lever, Left,F – G	1		H100 – 0207
P20	Shield Plate, LCD	1		H100 – 0195
P21	Protector, Cable	1		K100 – 0196
P22	Cushion, Cable	1		K100 – 0197
P23	Cover, Cable, Fawn – Grey	1		K100 – 0198
P24	Yoke, Right	1		K100 – 0199
P25	Yoke, Left	1		K100 – 0203
P26	Lock Button, Fawn – Grey	2		K100 – 0204

REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
P27	Frame, LCD, Fawn – Grey	1		K100 – 0205
P28	Case, Top, Fawn – Grey	1		G100 – 0208
	(With Battery Cishion)	1		
P29	Pin, Spring, Lever	2		K100 – 0210
P30	Spring, Lever	2		K100 – 0211
P31	Cover EXPANSION, F-G	1		H100 – 0212
P32	Cover MODEM, F-G	1		H100 – 0213
P33	Rear Cover, Fawn-Grey	1		K100 – 0214
P34	Plate, Name	1		H100 – 0215
P35	Foot, Rubber, Black	2		K100 – 0216
P36	Label, Rating & FCC	1		K100 – 0217
P37	Cover, Battery, Fawn-Grey	1		K100 – 0221
P38	Seal, Screw, Lever, F-G	2		K100 – 0219
P39	Seal, Screw, Case Bottom, Black	2		K100 – 0218
P39'	Seal, Rubber, Screw, Case, bottom Black	4		K100 – 0247
P40	Screw, Pan Head M1.7 × 3	1		K071 – 3202455
P41	Screw, Pan Head M2.0 × 4	4		K071 – 3219189
P42	Screw, Binding M2.6 × 4	2		K071 – 3000507
P43	Screw, Binding M3.0 × 5	2		K071 – 3000795
P44	Screw, Countersunk M3.0x5	2		K071 – 3600815
P45	Screw, Flat Head M3.0 × 6	7		K071 – 3000834
P46	Screw, Binding M3.0 × 8, Black	8		K071 – 3002832
P47	Screw, Tapping M3.0 × 8	3		K071 – 3000888
P48	Screw, Binding M3.0 × 10	6		K071 – 3002796
P49	Screw, Tapping M3.0 × 12	5		K071 – 3000651
P50	Screw, Binding M3.0 × 8	18		K071 – 3000832
P51	Spring, Lock Button	2		K100 – 0225
P52	Clip, Connector	1		K100 – 0226
P53	Tape, Conductive	2		K100 – 0227
P54	Spacer, Memory	1		K100 – 0228
P55	Cushion, Cover, Power Source	4		K100 – 0229
P56	Not used			
P57	Screw, Pan Head With Spring Washer & Washer M2.6 × 5	4		K071 – 3200513
P58	Screw, Pan Head With Spring Washer, M3.0 × 6	4		K071 – 3200639
P59 – 60	Not used			
P61	Pillar, SUB PCB	1		K100 – 0224
P62	Not used			
P63	Retainer, Screw	4		K100 – 0235
P64	Not used			
P65	Cushion, LCD	1		K100 – 0245
P66	Patch, Switch, Black	1		K100 – 0231

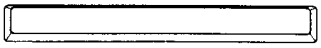
Keyboard Unit Assembly

REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
KEYBOARD	KEYBOARD, U.S.A.	1		20305 – 020
K1-76	Key Switch, KLT	76		56 – 9937D
K77	PCB, Key Switch	1		56 – A354A
K78	JUMPER WIRE	7		56 – 0123H
K79	Crank Holder LS	14		56 – 0926A
K80	Crank Shaft For SpaceKey Top	1		56 – 7837A
K81	Crank Shaft For Wide Key Tops	5		56 – 3199A
K82	Crank Shaft For Enter Key Top	1		56 – 1090A
K83	Spring Guide For Enter Key	2		56 – 7266A
K84	Spring For Space Key	2		56 – 7955D
K85	Crank Guide For Wide Key Tops	12		56 – 3200A
K86	Crank Guide For Space key Tops	2		56 – 8837A
K87	Cloth, Keyboard, Black	1		56 – A340A
K88	Connector	2		56 – 4099G
K89	Tape, Double – Sided	1		56 – 2016

REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
KEY TOPS				
K90	Set, Keytops	1		56 – A518
K90 – 1	Key Top  ,	1		
K90 – 2	Key Top  ,	1		
K90 – 3	Key Top  ,	1		
K90 – 4	Key Top  ,	1		
K90 – 5	Key Top  ,	1		
K90 – 6	Key Top  ,	1		
K90 – 7	Key Top  ,	1		
K90 – 8	Key Top  ,	1		
K90 – 9	Key Top  ,	1		
K90 – 10	Key Top  ,	1		
K90 – 11	Key Top  ,	1		
K90 – 12	Key Top  ,	1		
K90 – 13	Key Top  ,	1		
K90 – 14	Key Top  ,	1		
K90 – 15	Key Top  ,	1		
K90 – 16	Key Top  ,	1		
K90 – 17	Key Top  ,	1		
K90 – 18	Key Top  ,	1		
K90 – 19	Key Top  ,	1		
K90 – 20	Key Top  ,	1		
K90 – 21	Key Top  ,	1		
K90 – 22	Key Top  ,	1		
K90 – 23	Key Top  ,	1		
K90 – 24	Key Top  ,	1		

REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
K90 – 25	Key Top [P],	1		
K90 – 26	Key Top [I],	1		
K90 – 27	Key Top [U],	1		
K90 – 28	Key Top  ,	1		
K90 – 29	Key Top [Ctrl],	1		
K90 – 30	Key Top [A],	1		
K90 – 31	Key Top [S],	1		
K90 – 32	Key Top [D],	1		
K90 – 33	Key Top [F],	1		
K90 – 34	Key Top [G],	1		
K90 – 35	Key Top [H],	1		
K90 – 36	Key Top [J],	1		
K90 – 37	Key Top [K],	1		
K90 – 38	Key Top [L],	1		
K90 – 39	Key Top [;],	1		
K90 – 40	Key Top [Shift],	1		
K90 – 41	Key Top [Shift], Left	1		
K90 – 42	Key Top [Z],	1		
K90 – 43	Key Top [X],	1		
K90 – 44	Key Top [C],	1		
K90 – 45	Key Top [V],	1		
K90 – 46	Key Top [B],	1		
K90 – 47	Key Top [N],	1		
K90 – 48	Key Top [M],	1		
K90 – 49	Key Top [<],	1		

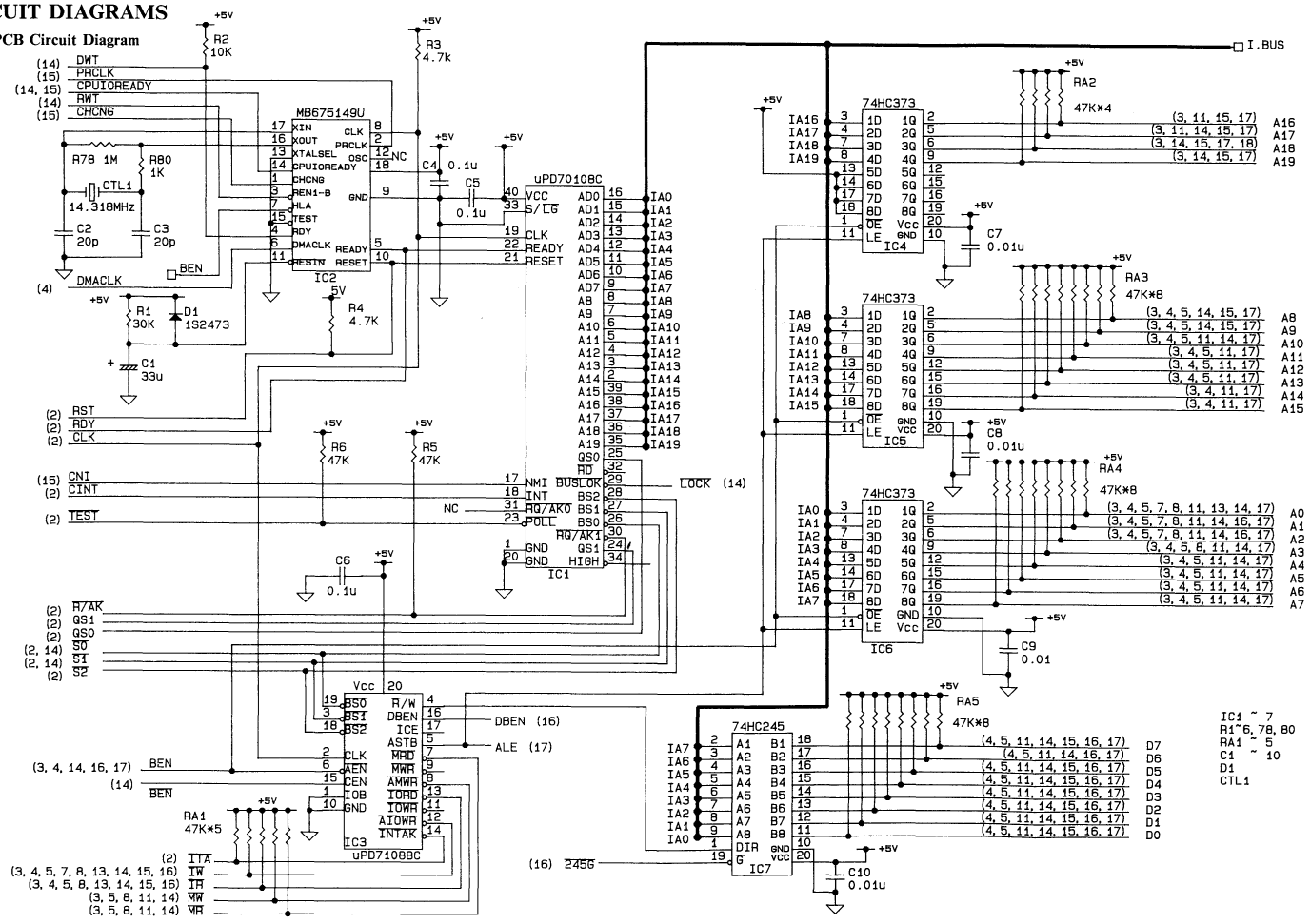
REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
K90 – 50	Key Top  ,	1		
K90 – 51	Key Top  ,	1		
K90 – 52	Key Top  , Right	1		
K90 – 53	Key Top  ,	1		
K90 – 54	Key Top  ,	1		
K90 – 55	See K91			
K90 – 56	Key Top  ,	1		
K90 – 57	Key Top  ,	1		
K90 – 58	Key Top  ,	1		
K90 – 59	Key Top  ,	1		
K90 – 60	Key Top  ,	1		
K90 – 61	Key Top  ,	1		
K90 – 62	Key Top  ,	1		
K90 – 63	Key Top  ,	1		
K90 – 64	Key Top  ,	1		
K90 – 65	Key Top  ,	1		
K90 – 66	Key Top  ,	1		
K90 – 67	Key Top  ,	1		
K90 – 68	Key Top  ,	1		
K90 – 69	Key Top  ,	1		
K90 – 70	Key Top  ,	1		
K90 – 71	Key Top  ,	1		
K90 – 72	Key Top  ,	1		
K90 – 73	Key Top  ,	1		
K90 – 74	Key Top  ,	1		

REF.NO.	DESCRIPTION	Q'TY	RS PART NO.	MFR'S PART NO.
K90 – 75	Key Top  ,	1		
K90 – 76	Key Top  ,	1		
K91	Space key  Off white	1		56 – 5466H
KD1 – 76	Diode,Silicon 1S2473	76		56 – 0224C

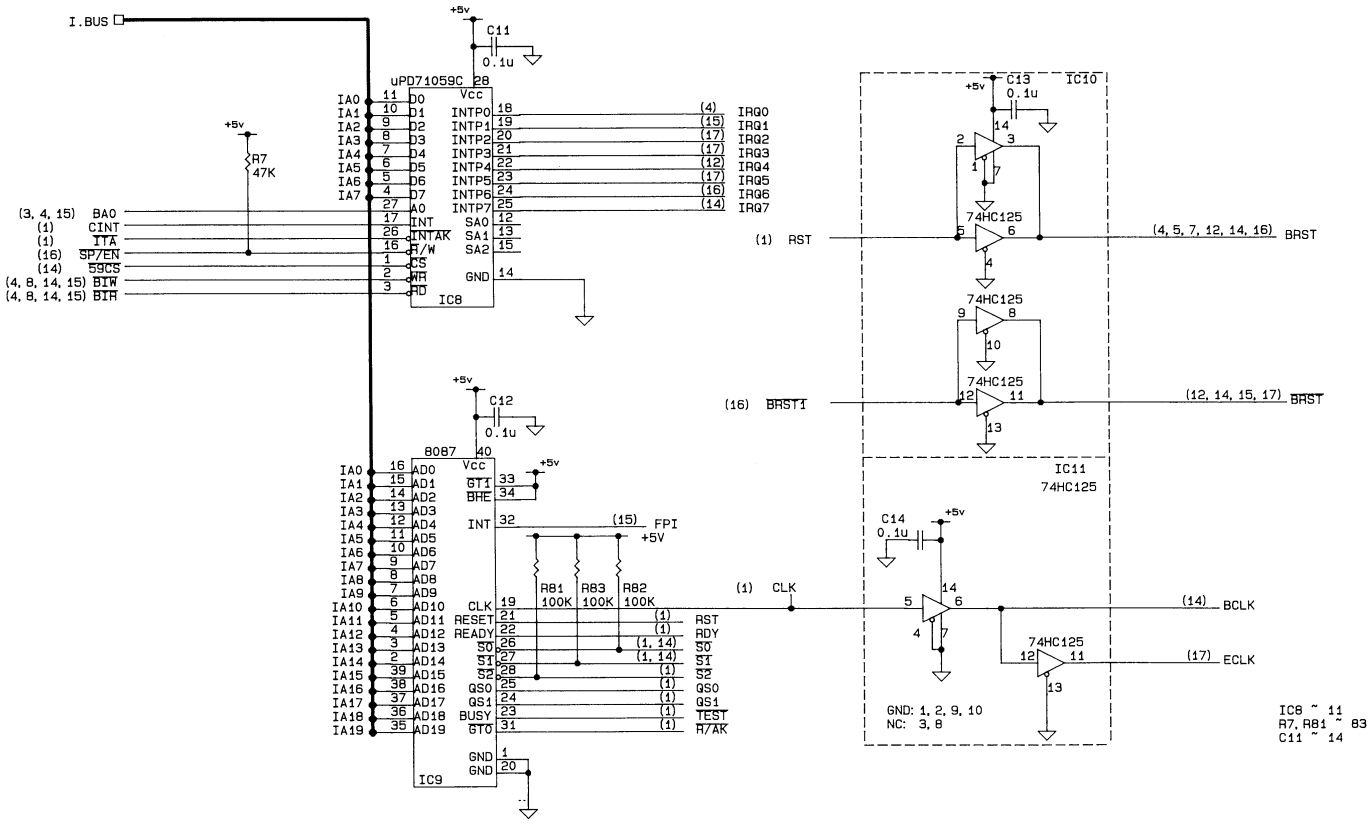
VII. CIRCUIT DIAGRAMS

VII-1. Main PCB Circuit Diagram

CPU

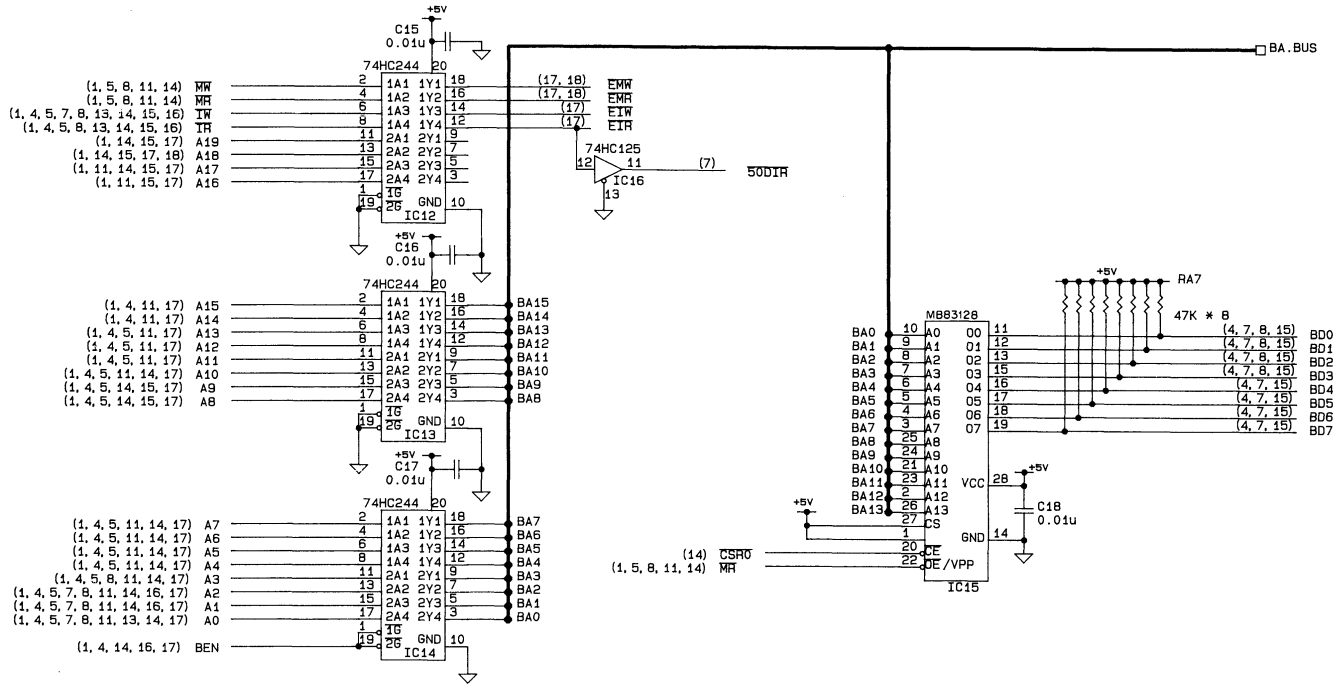


NO. 1

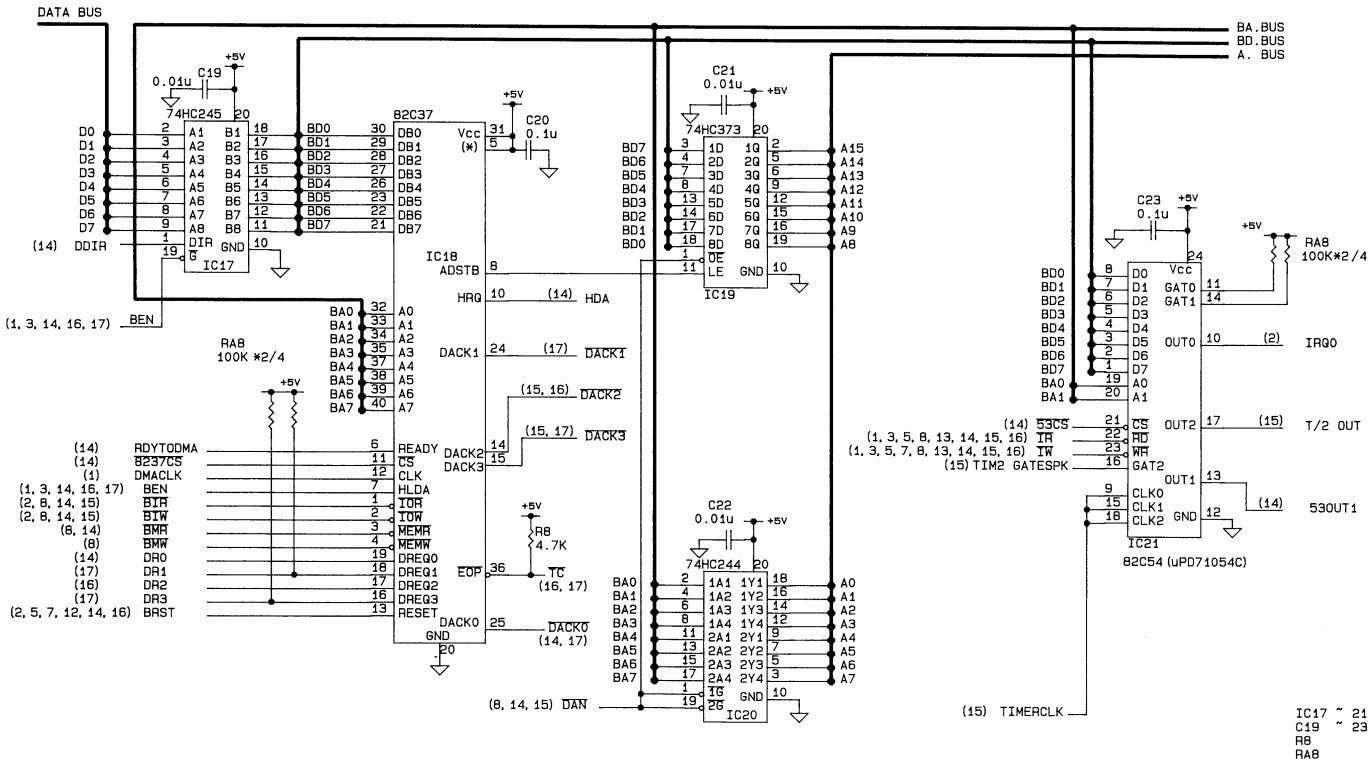


NO. 2

ROM

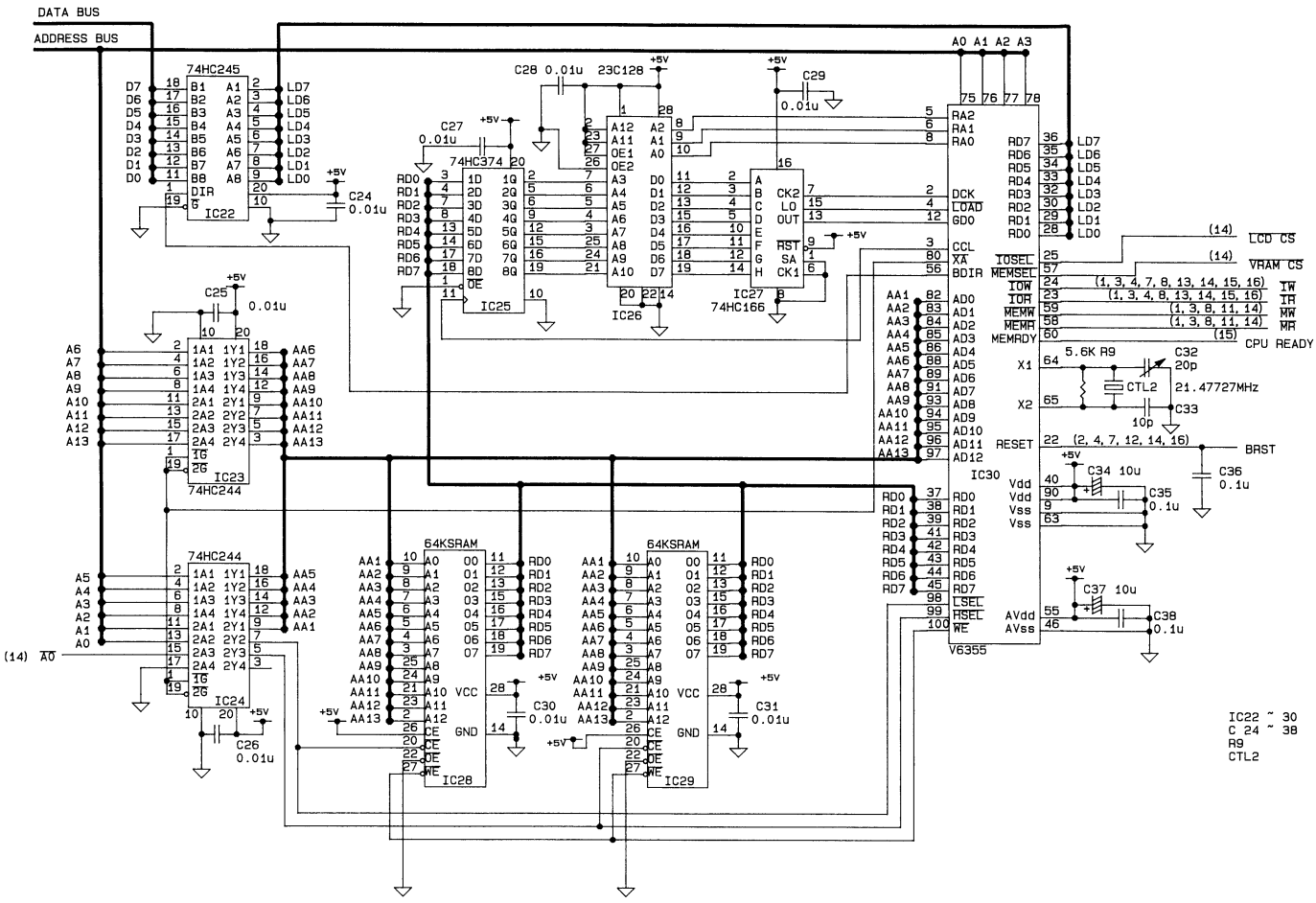


NO. 3



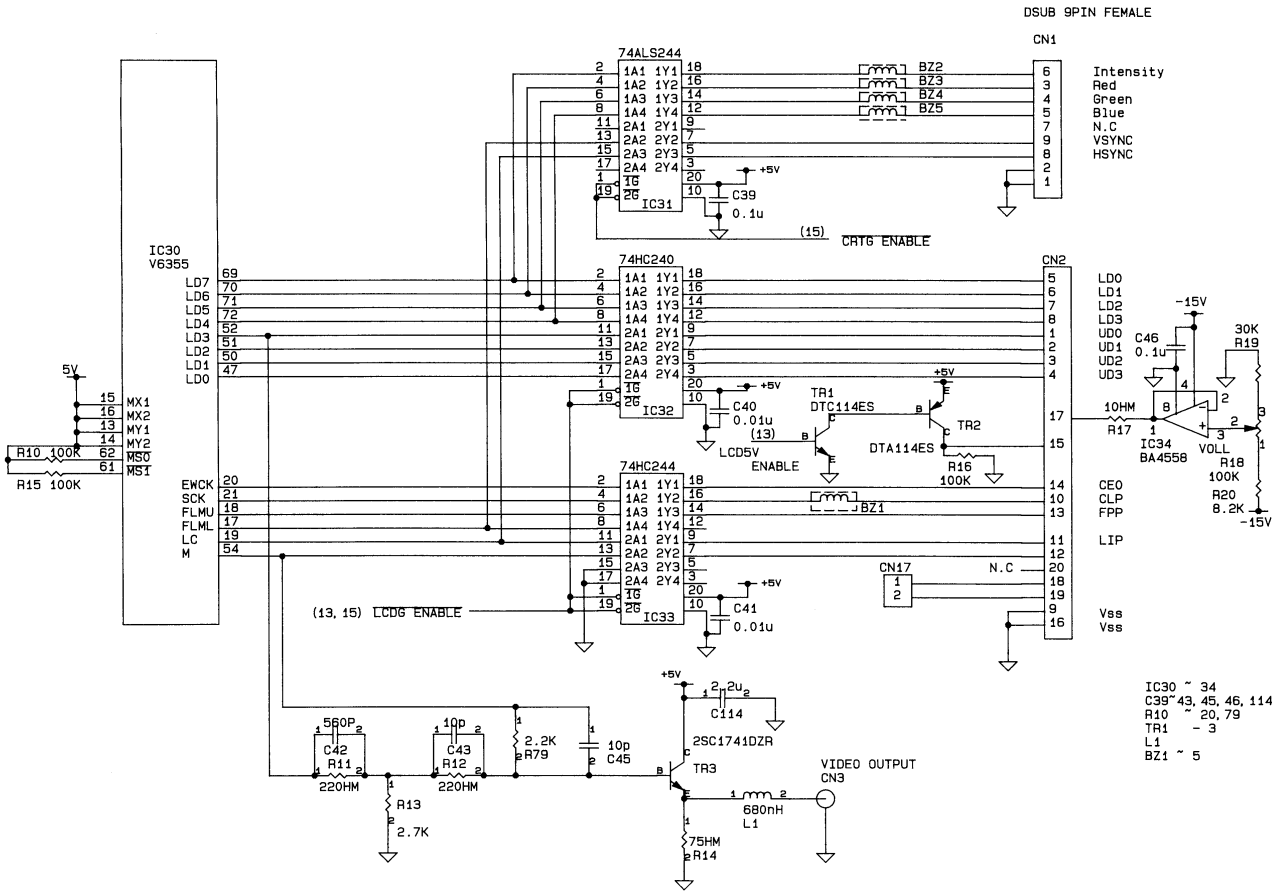
NO. 4

LCD, CRT



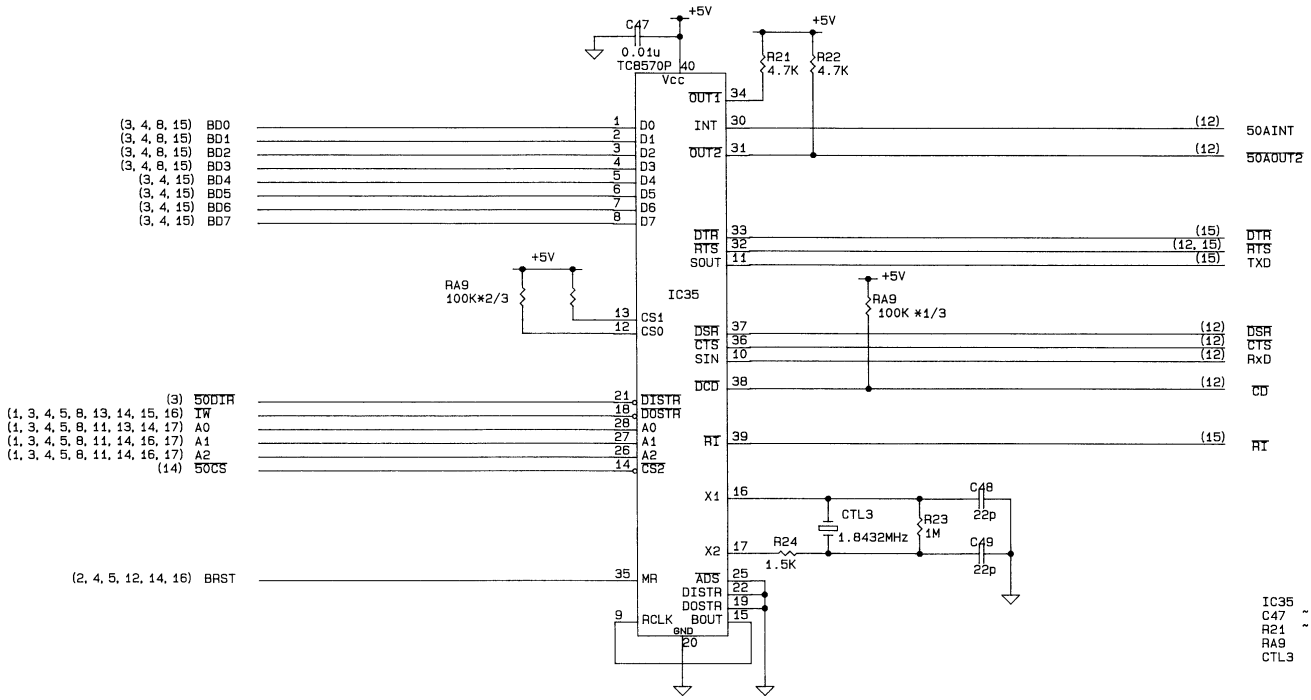
NO. 5

7-5

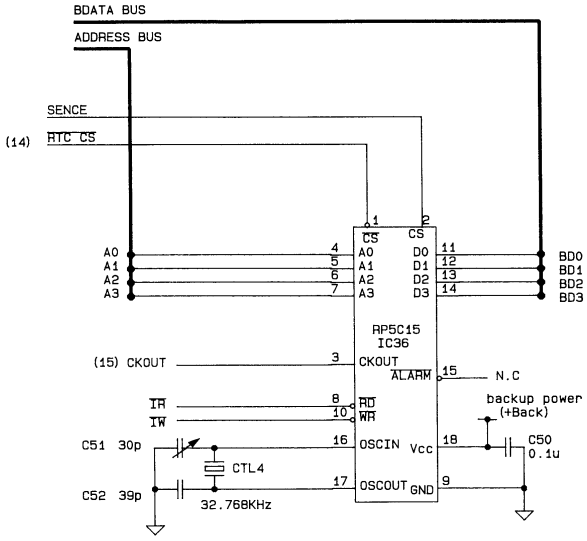


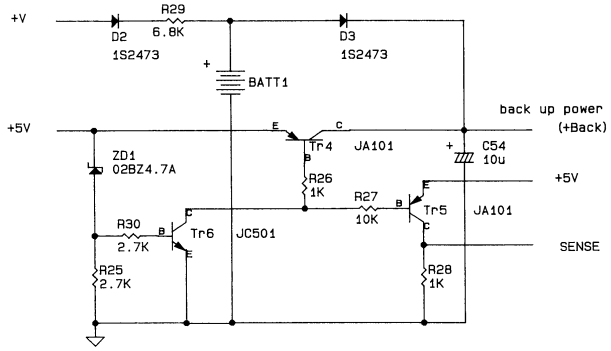
NO. 6

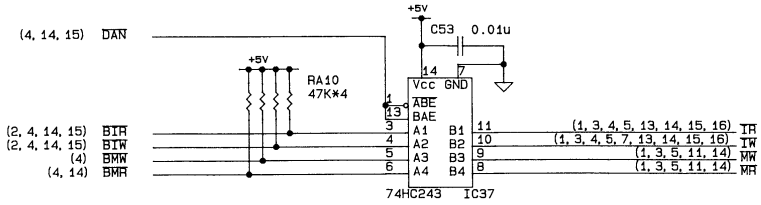
UART



RTC, Back up





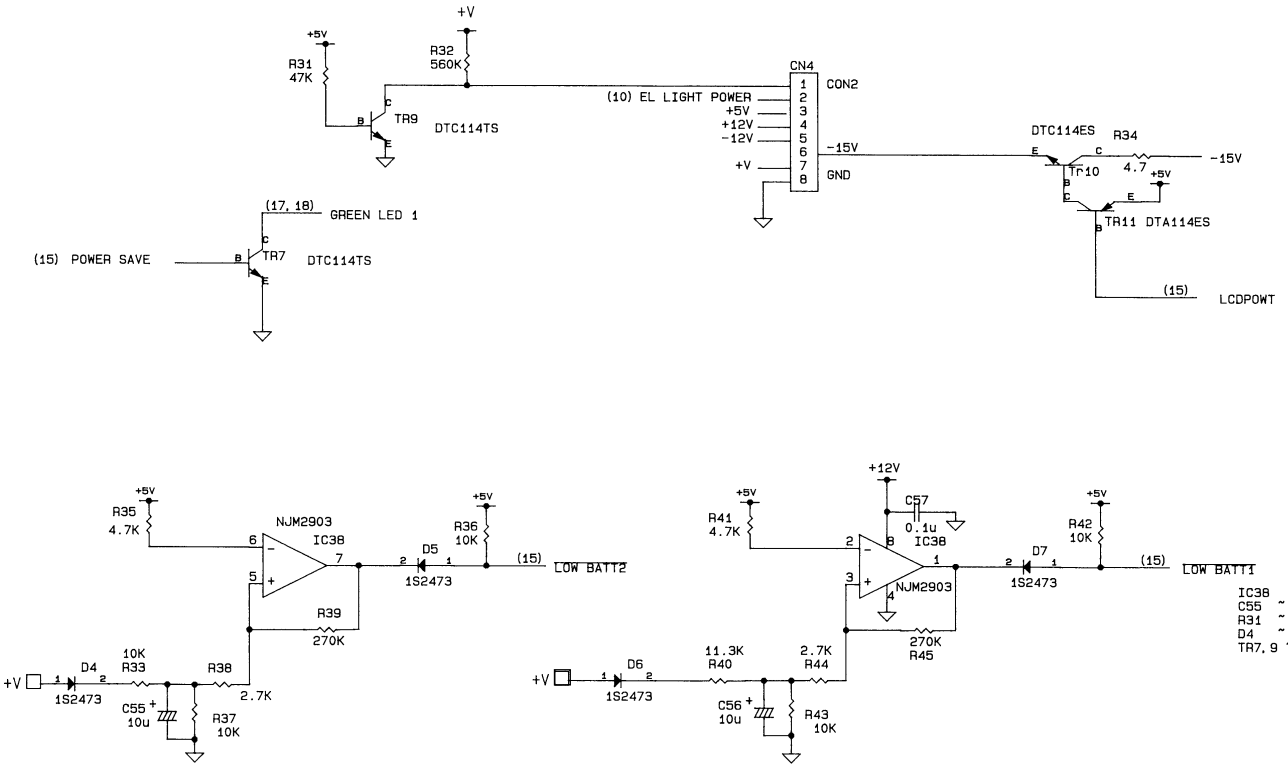


IC36, 37
C50 ~ 54
R25 ~ 30
RA10
TR4 ~ 6
D2 ~ 3
ZD1
CTL4
BATT1

NOTE : backup power = 3.6 ~ 4.4V
: +V = 12 ~ 13V

NO. 8

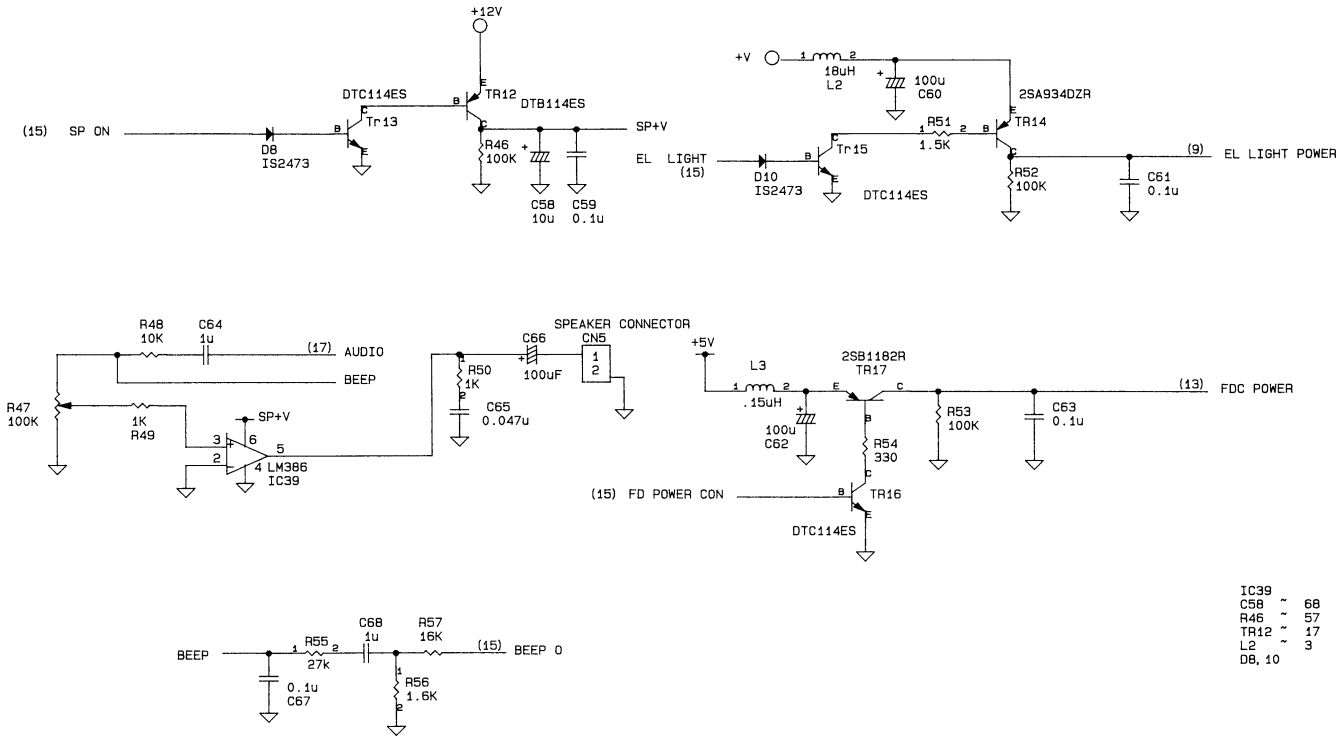
Low Battery, etc



[**NOTE** : +V = 12 ~ 13V]

NO. 9

BEEP, (SP, EL, FDC) Power Control

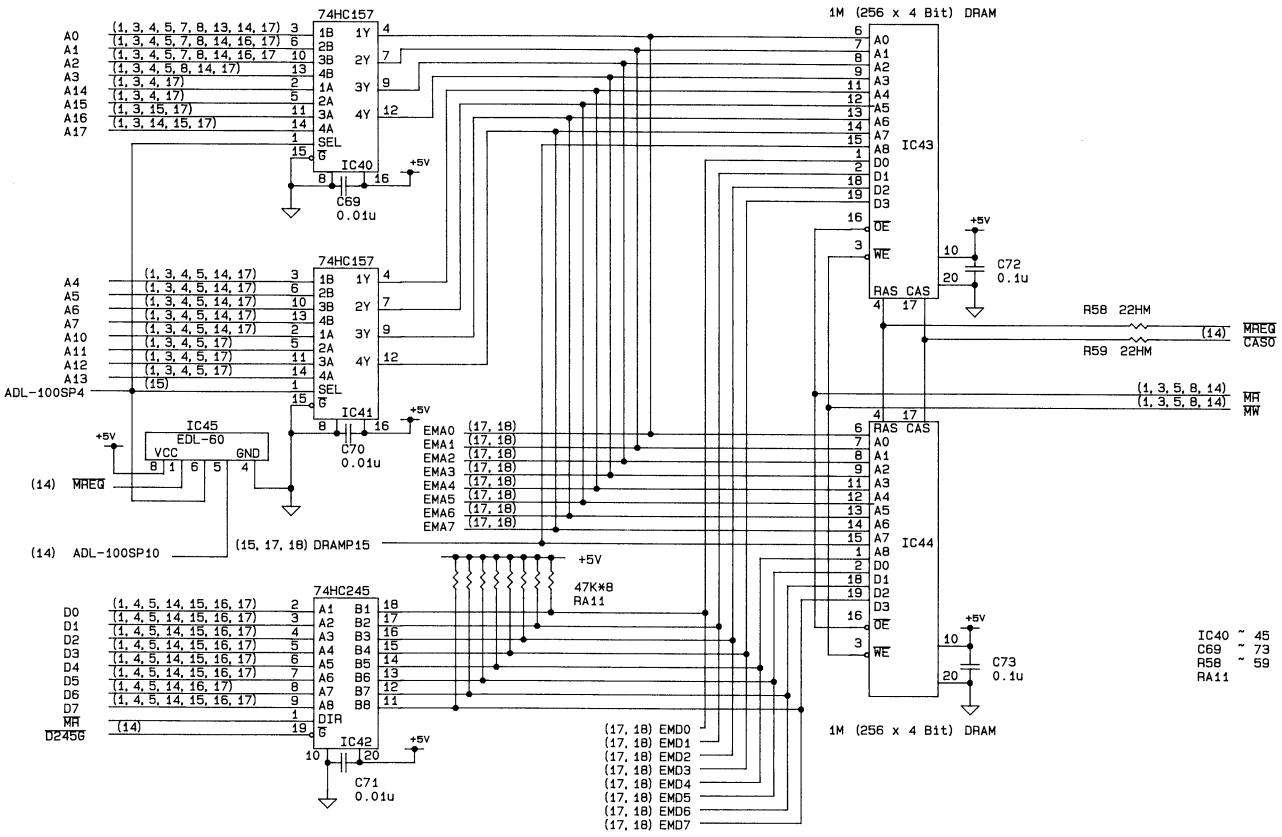


IC39
C58 ~ 68
R46 ~ 57
TR12 ~ 17
L2 ~ 3
D8, 10

[**NOTE** : +V = 12 ~ 30V]

NO. 10

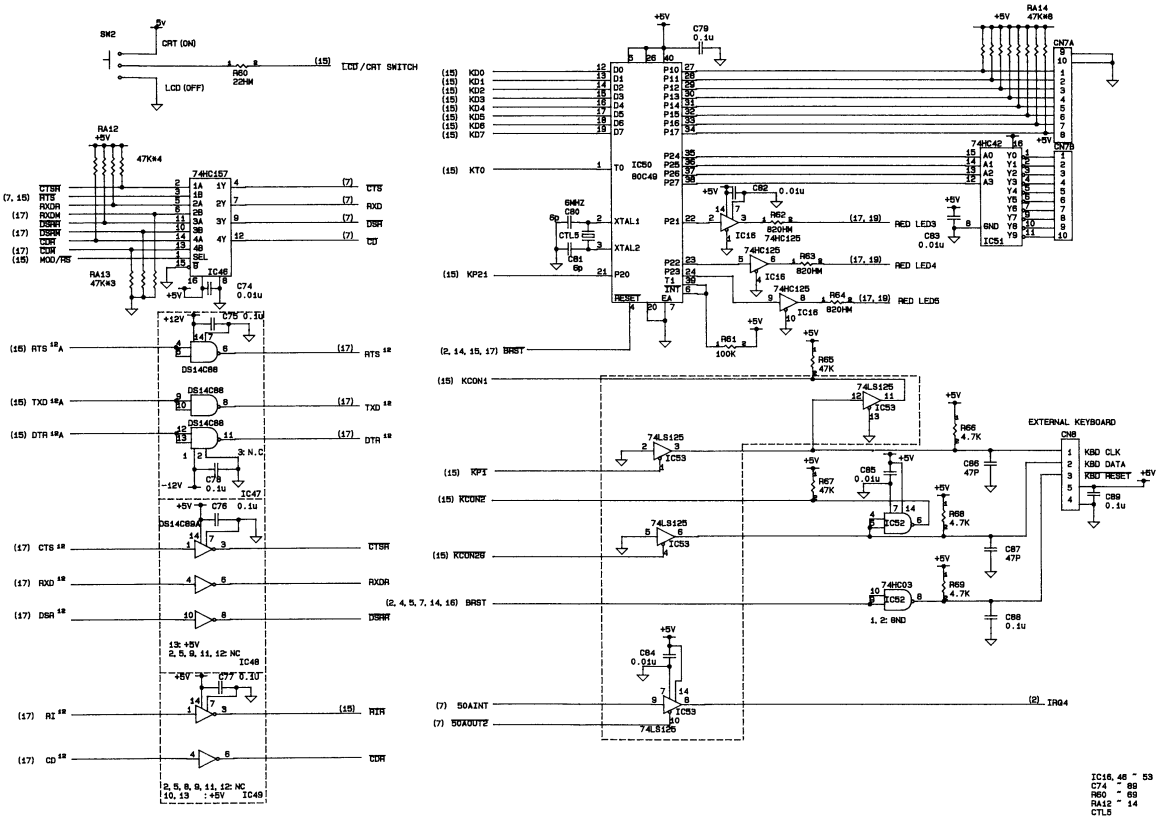
RAM



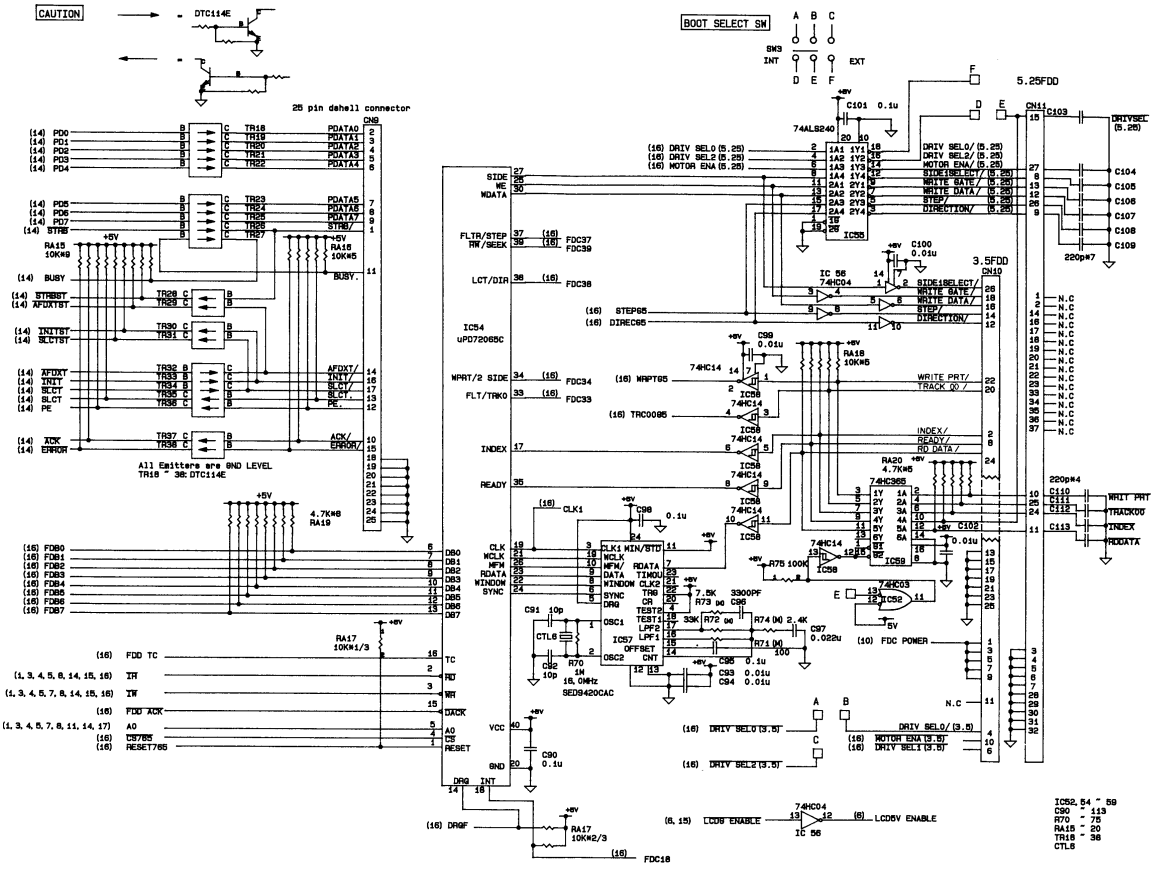
NO. 11

7-11

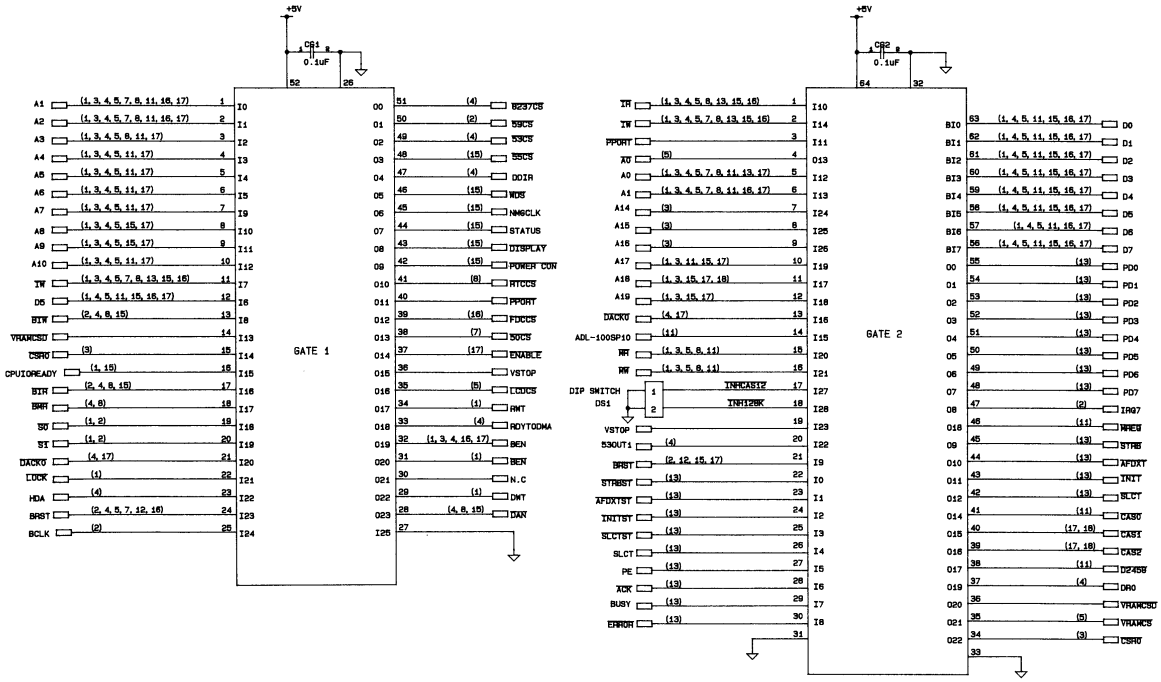
Keyboard, Serial Interface



NO. 12

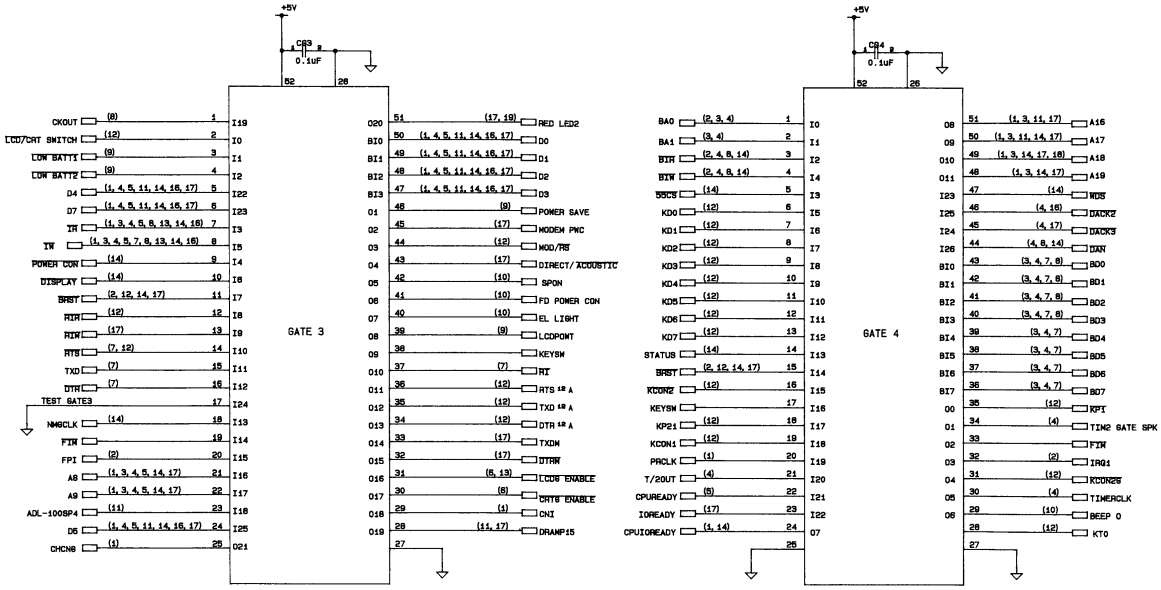


Gate Arrays Pin Out (Gate 1, Gate 2)

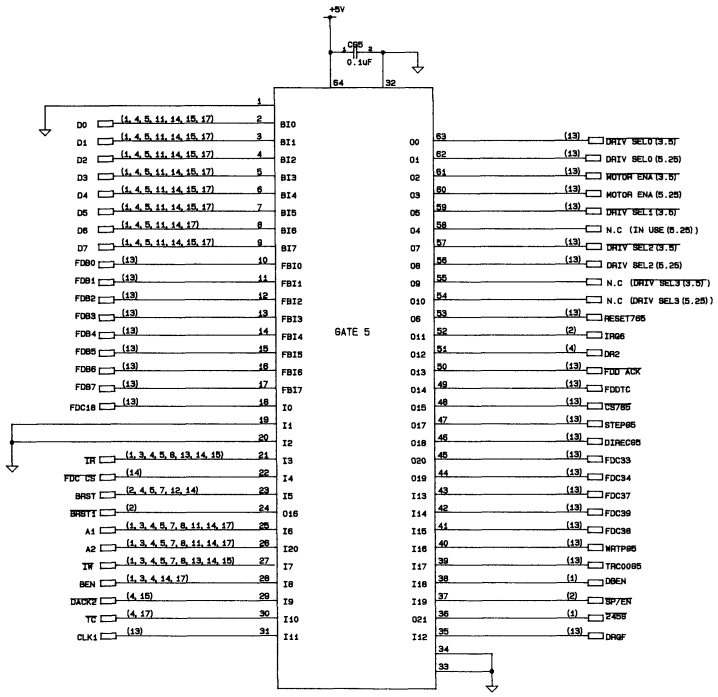


NO. 14

Gate Arrays Pin Out (Gate 3, Gate 4)



Gate Array Pin Out (Gate 5)



NO. 16

Connector

EXPANSION INTERFACE PORT

CN12

N.C	1	
+5V	2	
ENABLE	3	(14)
N.C	4	
N.C	5	
DACK0	6	(4, 14)
IRQ3	7	(2)
N.C	8	
GND	9	
A0	10	(1, 3, 4, 5, 7, 8, 11, 13, 14)
A1	11	(1, 3, 4, 5, 7, 8, 11, 14, 16)
A2	12	(1, 3, 4, 5, 7, 8, 11, 14, 16)
A3	13	(1, 3, 4, 5, 8, 11, 14)
A4	14	(1, 3, 4, 5, 11, 14)
A5	15	(1, 3, 4, 5, 11, 14)
A6	16	(1, 3, 4, 5, 11, 14)
A7	17	(1, 3, 4, 5, 11, 14)
GND	18	
A8	19	(1, 3, 4, 5, 14, 15)
A9	20	(1, 3, 4, 5, 14, 15)
A10	21	(1, 3, 4, 5, 11, 14)
A11	22	(1, 3, 4, 5, 11)
A12	23	(1, 3, 4, 5, 11)
A13	24	(1, 3, 4, 5, 11)
A14	25	(1, 3, 4, 11)
A15	26	(1, 3, 4, 11)
GND	27	
A16	28	(1, 3, 11, 15)
A17	29	(1, 3, 11, 14, 15)
A18	30	(1, 3, 14, 15, 16)
A19	31	(1, 3, 14, 15)
D0	32	(1, 4, 5, 11, 14, 15, 16)
D1	33	(1, 4, 5, 11, 14, 15, 16)
D2	34	(1, 4, 5, 11, 14, 15, 16)
D3	35	(1, 4, 5, 11, 14, 15, 16)
GND	36	
D4	37	(1, 4, 5, 11, 14, 15, 16)
D5	38	(1, 4, 5, 11, 14, 15, 16)
D6	39	(1, 4, 5, 11, 14, 16)
D7	40	(1, 4, 5, 11, 14, 15, 16)
$\overline{EMW}$	41	(3, 18)
$\overline{EMR}$	42	(3, 18)
GND	43	
$\overline{EIW}$	44	(3)
$\overline{EIR}$	45	(3)
$\overline{TC}$	46	(4, 16)
ALE	47	(1)
$\overline{BRST}$	48	(2, 12, 14, 15)
$\overline{DACK1}$	49	(4)
IRQ2	50	(2)
GND	51	
+5V	52	
ECLK	53	(2)
IRQ5	54	(2)
DR3	55	(4)
$\overline{DACK3}$	56	(4, 15)
BEN	57	(1, 3, 4, 14, 16)
DR1	58	(4)
IOREADY	59	(15)
GND	60	

SERIAL PORT

CN13

CD [12]	1	(12)
RXD [12]	2	(12)
TXD [12]	3	(12)
DTR [12]	4	(12)
GND	5	
DSR [12]	6	(12)
RTS [12]	7	(12)
CTS [12]	8	(12)
RI [12]	9	(12)

MEMORY CONNECTOR

CN14

EMA0	1	(11, 18)
EMA1	2	(11, 18)
EMA2	3	(11, 18)
EMA3	4	(11, 18)
EMA4	5	(11, 18)
EMA5	6	(11, 18)
EMA6	7	(11, 18)
EMA7	8	(11, 18)
DRAMP15	9	(11, 15, 18)
EMD0	10	(11, 18)
EMD1	11	(11, 18)
EMD2	12	(11, 18)
EMD3	13	(11, 18)
EMD4	14	(11, 18)
EMD5	15	(11, 18)
EMD6	16	(11, 18)
EMD7	17	(11, 18)
$\overline{EMR}$	18	(3, 18)
$\overline{EMW}$	19	(3, 18)
$\overline{CAS1}$	20	(14, 18)
$\overline{CAS2}$	21	(14, 18)
A18	22	(1, 3, 14, 15, 18)
GND	23	
+5V	24	
GND	25	
+5V	26	

MODEM CONNECTOR

CN15

TXDM	1	(15)
RXDM	2	(12)
$\overline{DTRM}$	3	(15)
$\overline{DSRM}$	4	(12)
$\overline{CDM}$	5	(12)
$\overline{RIM}$	6	(15)
MODEM PWC	7	(15)
N.C	8	
AUDIO	9	(10)
DIRECT/ACOUSTIC	10	(15)
GND	11	
+5V	12	
GND	13	
+5V	14	
GND	15	
+12V	16	
GND	17	
-12V	18	
N.C	19	
N.C	20	

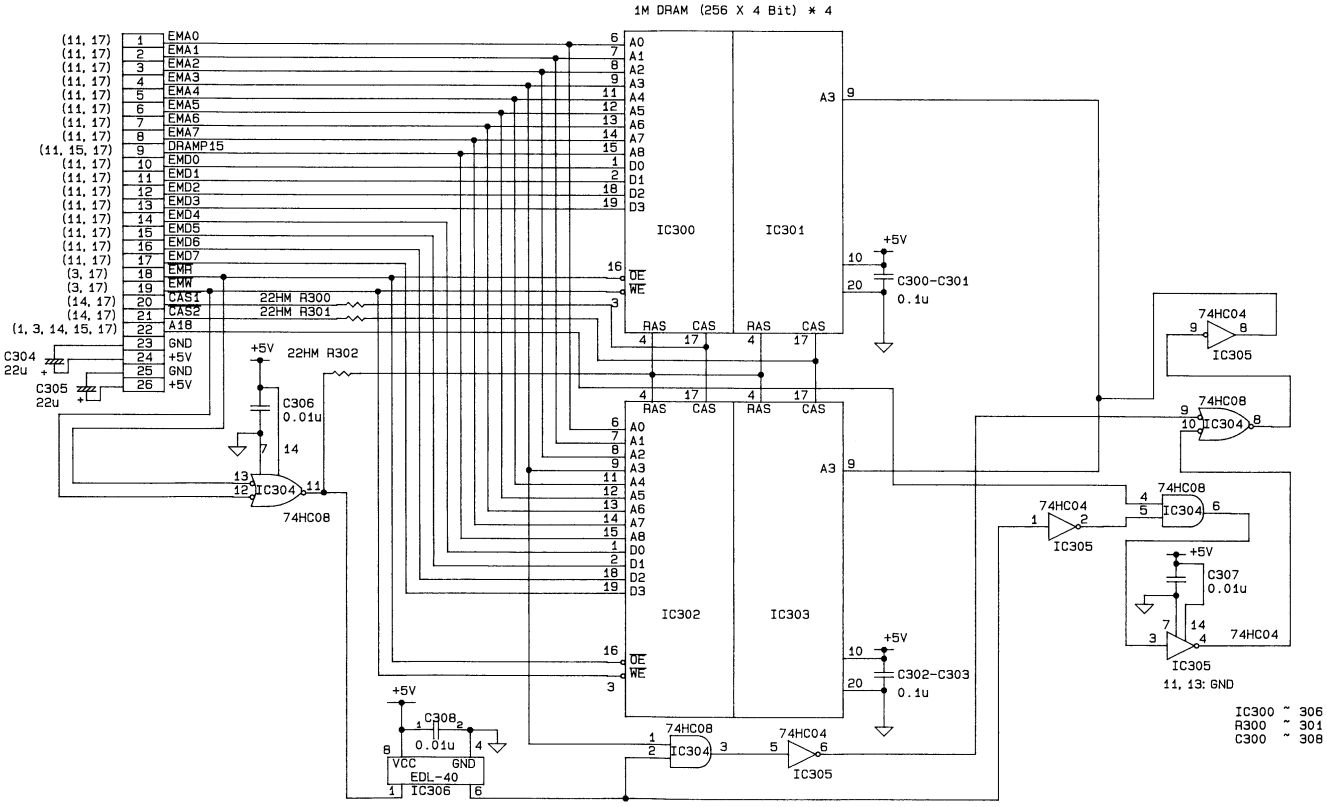
UPPER PCB CONNECTOR

CN16

GREEN LED1	1	(9, 19)
RED LED2	2	(15, 19)
RED LED3	3	(12, 19)
RED LED4	4	(12, 19)
RED LED5	5	(12, 19)
+5V	6	

VII-2. RAM PCB Circuit Diagram

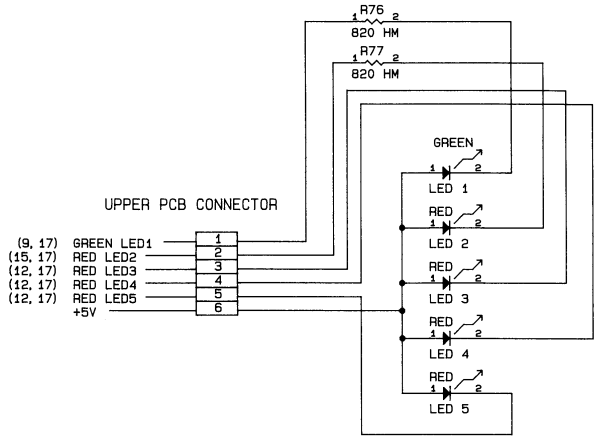
RAM



NO. 18

VII-3. LED (Upper) PCB Circuit Diagram

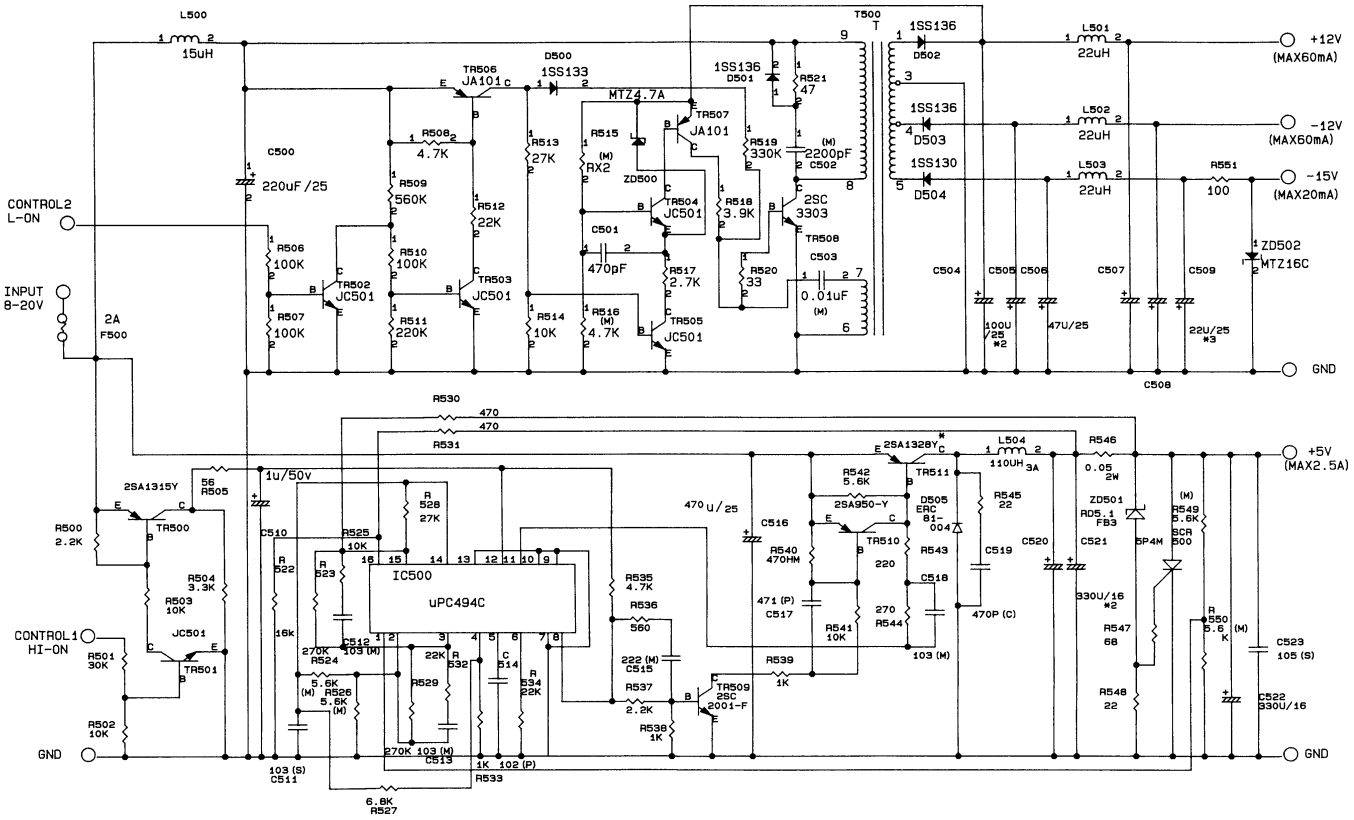
LED



LED 1 ~ 5
R 76 ~ 77

NO. 19

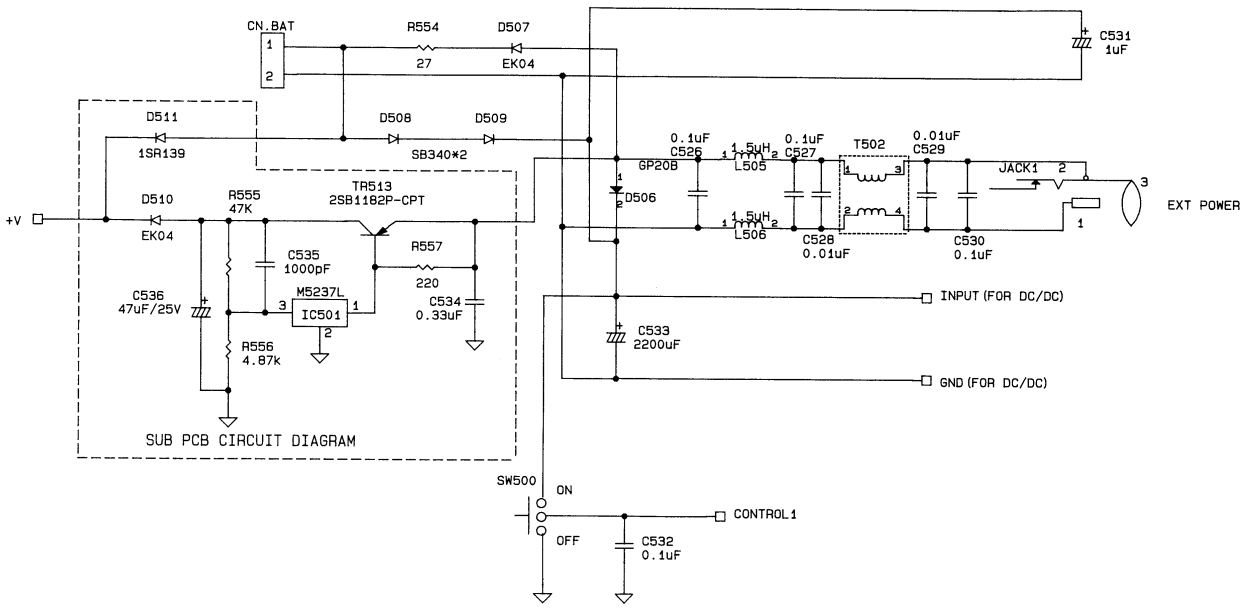
VII-4. Power PCB Circuit Diagram



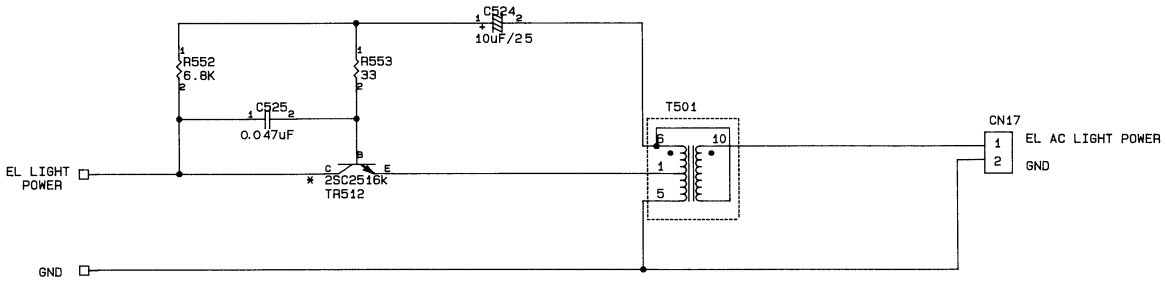
* This transistor needs Heatsink.
No. HS500

NO. 20

SUB PCB



[**NOTE** : +V = 12 ~ 13V]

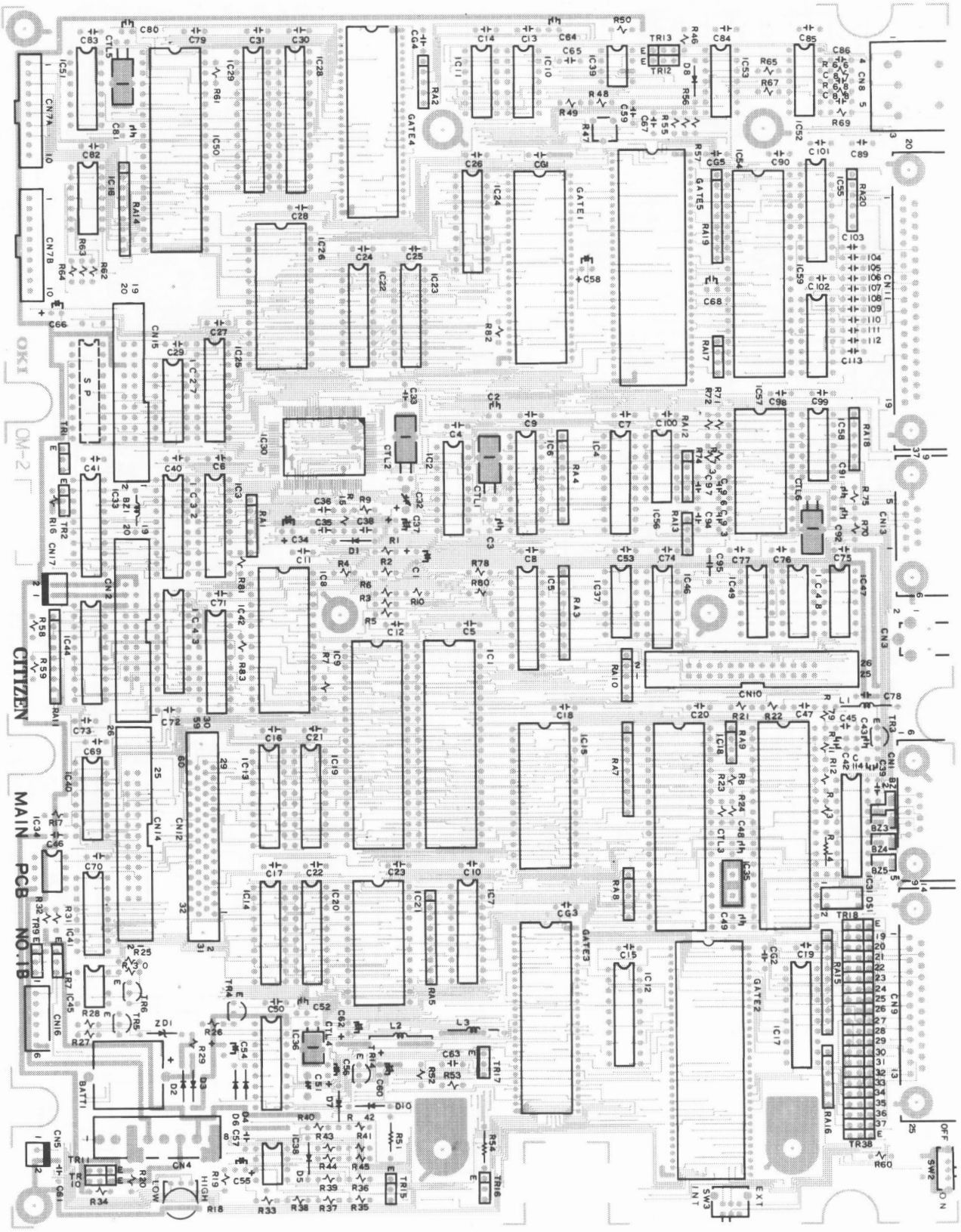


* This transistor needs Heatsink.
No. HS501

NO. 22

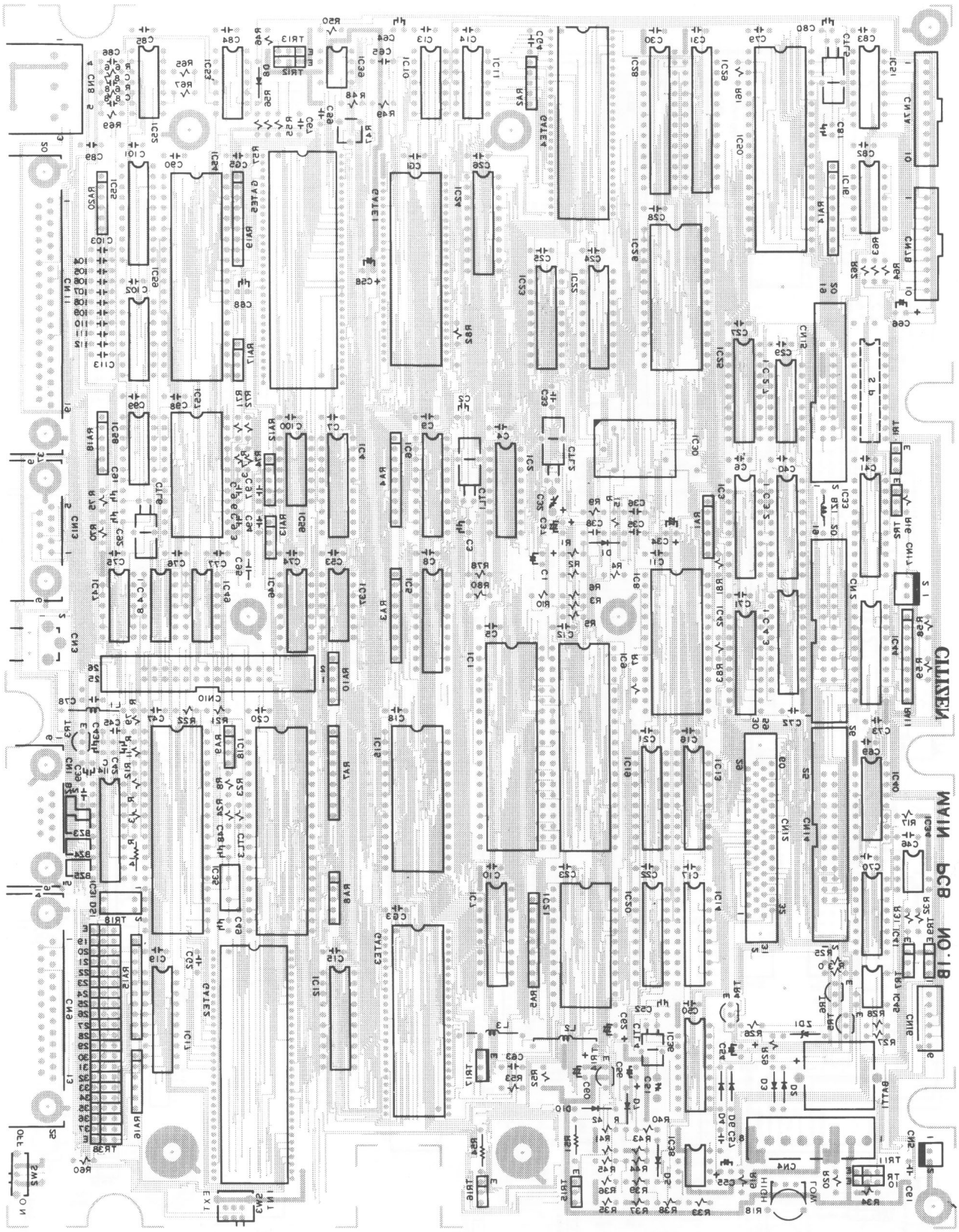
VIII. PCB VIEWS

VIII-1. Main PCB Views



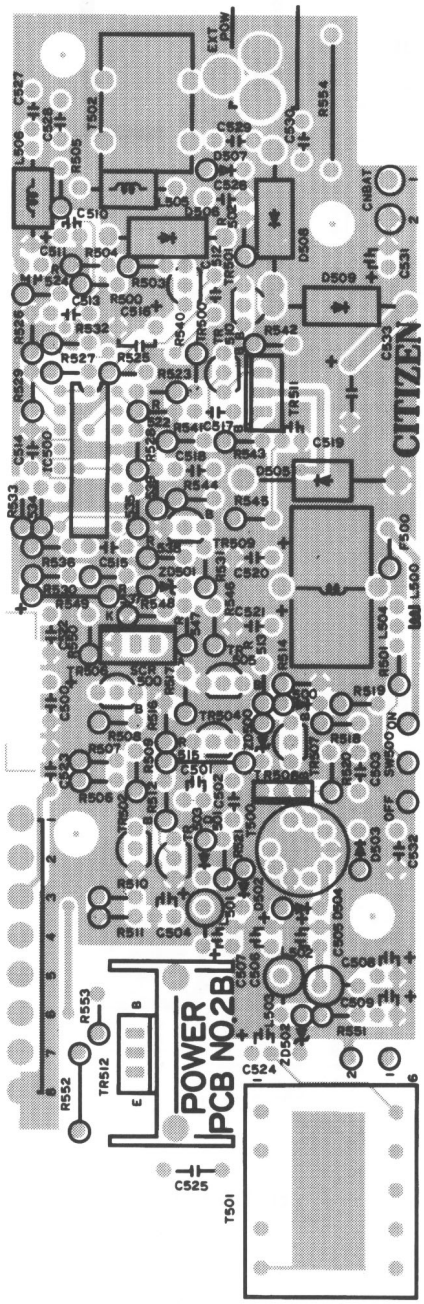
Top View

Main PCB Views

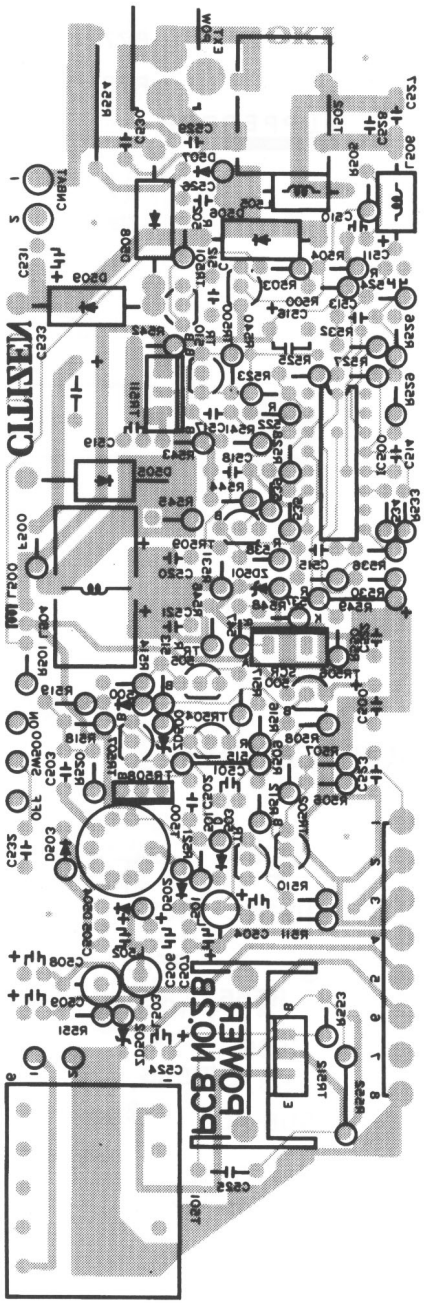


Bottom View

VIII-2. Power PCB Views

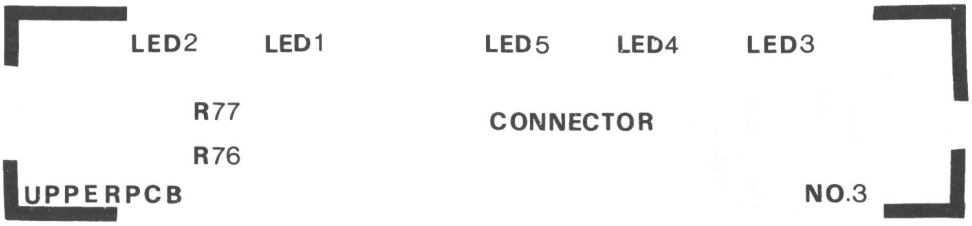


Top View



Bottom View

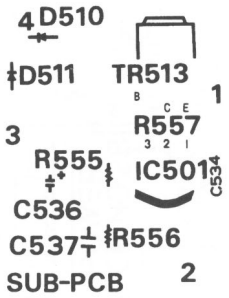
VIII-3. UPPER PCB (LED) Views



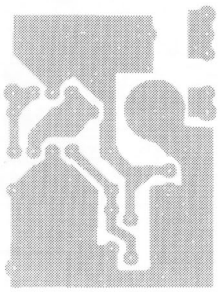
Top View

Bottom View

VIII-4. SUB PCB Views

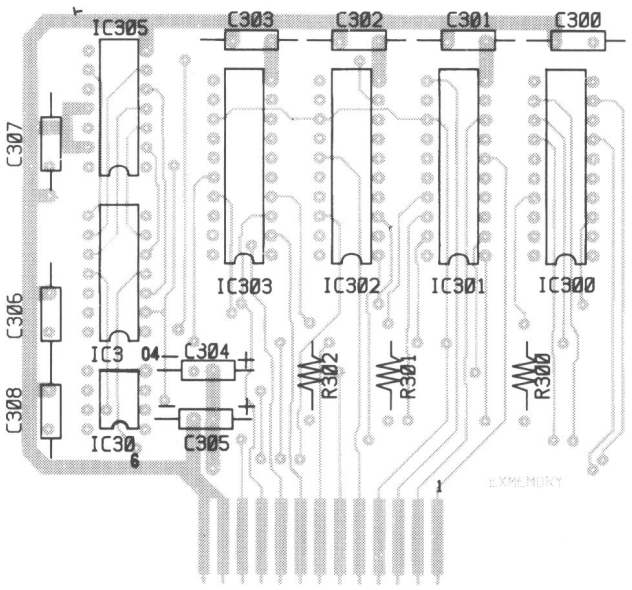


Top View

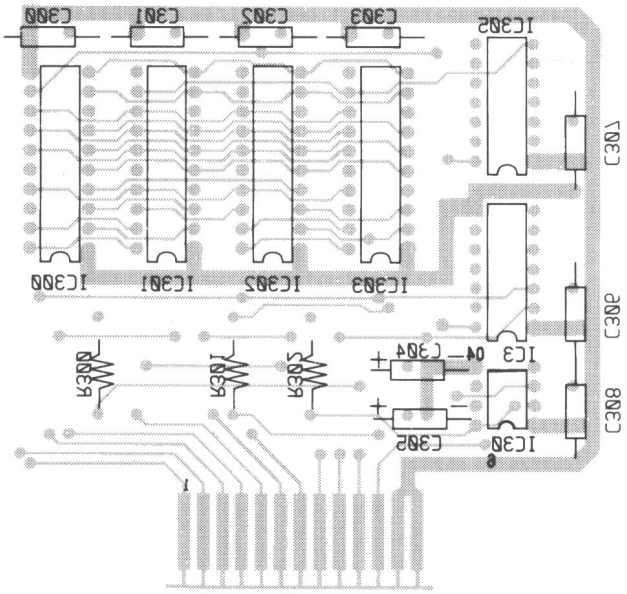


Bottom View

VIII-5. MEMORY PCB Views



Top View



Bottom View

APPENDICES

A. LCD SPECIFICATIONS

1. Application

This specification shall be applied to Dot Matrix LCD MODULE with EL back light CG-640200CG-0Z

2. Composition

Display type	: SIN, blue mode, transmissive negative display
Dot structure	: 640 × 200 Dot Graphic display
Driving method	: 1/100 duty Multiplex drive
Back light	: Electroluminescent (EL) white NEL-5LL-411-W
Surface texture	: Non-Glare

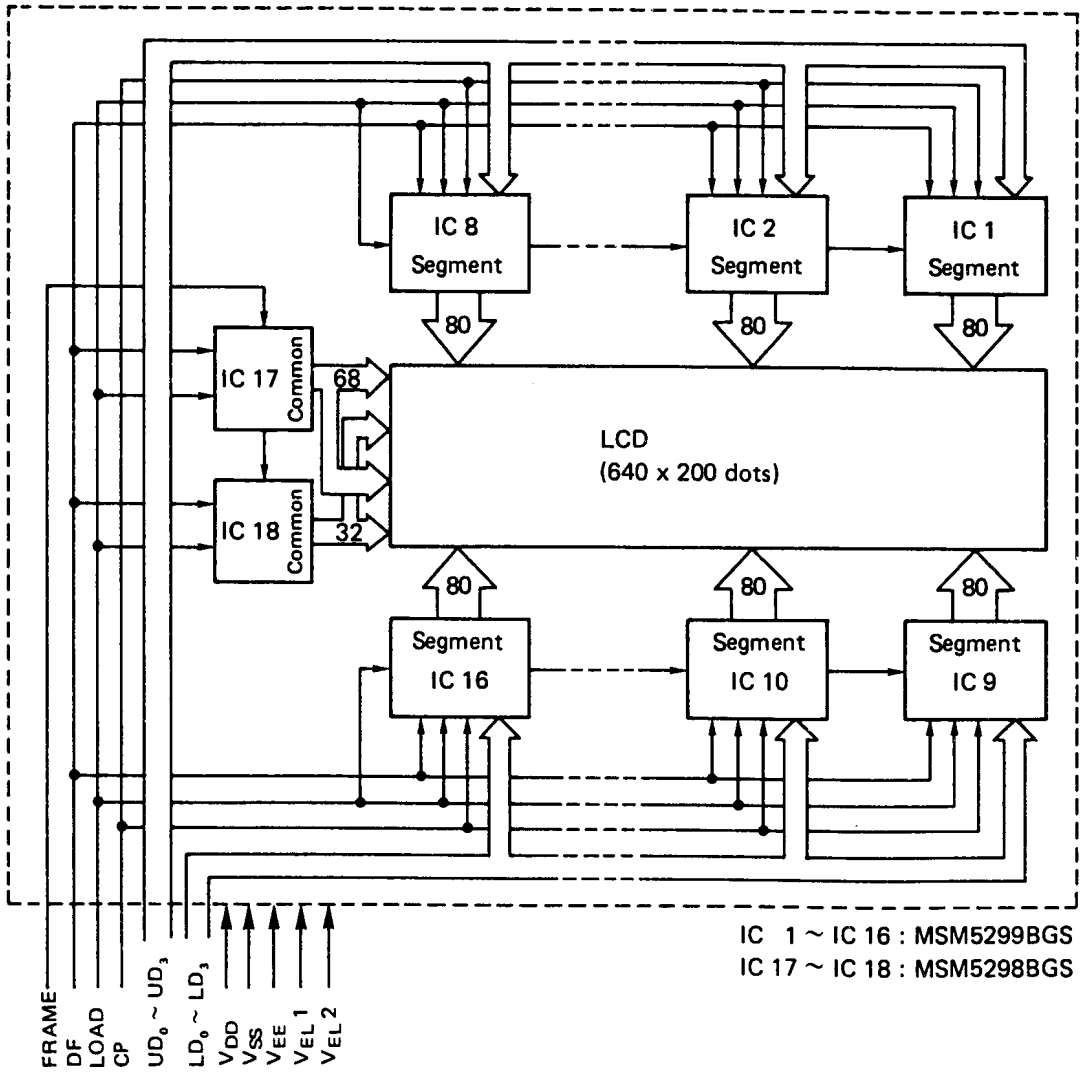


Figure A-1. Block Diagram

NOTES:
This does not incorporate any controller.
The V6355 (YAMAHA) is suitable as the controller IC.

3. Mechanical Specifications

Item	Dimensions	Unit
Module size	10.63 (W) × 6.1 (H) × 0.5 (D) max (270 × 154 × 12.2)	inches (mm)
Effective viewing area	9.76 (W) × 4.5 (H) (248 × 114)	inches (mm)
Weight	Approx 0.98 (440)	lbs (g)

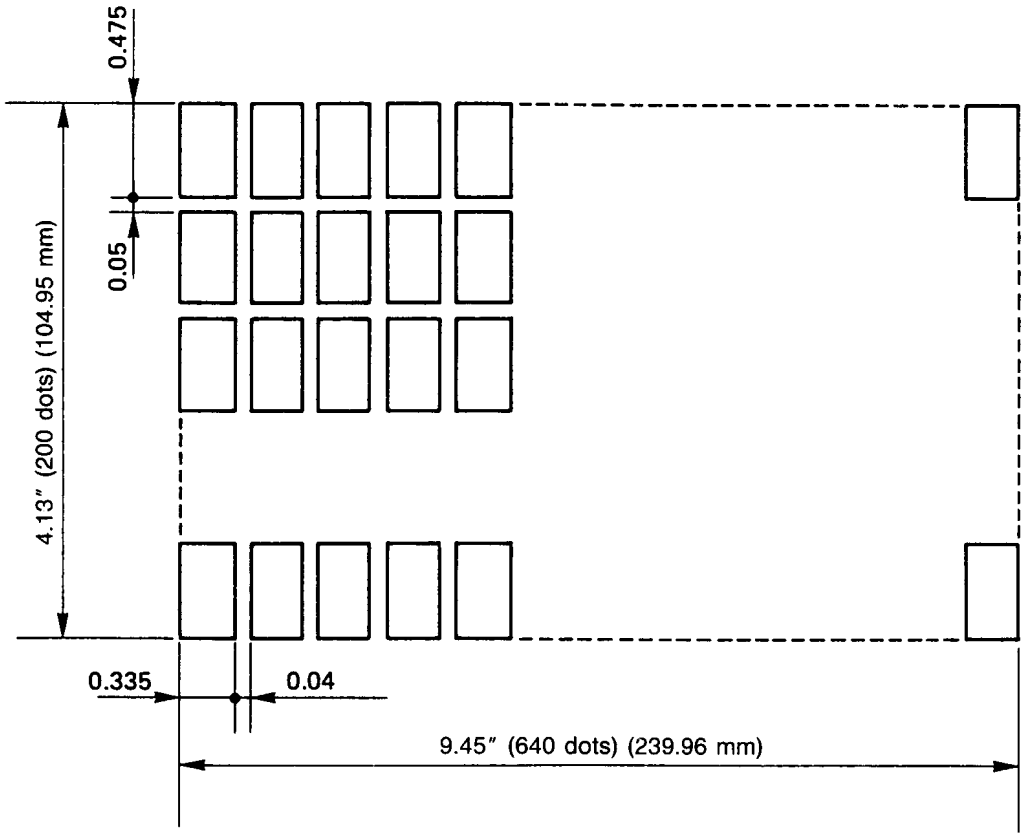


Figure A-2. Dot Dimensional Drawing

4. Electrical Specifications

4-1 Absolute Maximum Rating

Item	Symbol	Minimum	Maximum	Unit	Remarks
Supply voltage for logic circuit	V_{DD}-Vss	-0.3	+6.0	V	
Supply voltage for LCD driving	V_{DD}-V_{EE}	0	+30.0	V	
Supply voltage for EL back light	V_{EL}1-V_{EL}2	——	+ 150	ACVrms	
Supply frequency for EL back light	f_{EL}	——	+ 800	Hz	
Input voltage	V_{IN}	-0.3	V_{DD}+0.3	V	
Storage temperature	Tstg	-4 (-20)	140 (+60)	°F (°C)	
Operating tempreature	Topr	32 (0)	104 (+40)	°F (°C)	

4-2 Electrical Characteristics

(VSS=0V)

Item		Symbol	Test condition	Minmum	Typical	Maximum	Unit
Supply voltage for logic circuit		V_{DD}-Vss		4.5	5.0	5.5	V
Supply voltage for LCD driving		V_{DD}-V_{EE}		8.0	——	28.0	V
Supply voltage for EL back light		V_{EL}1-V_{EL}2		——	100	——	ACVrms
Supply frequency for EL back light		f_{EL}		——	400	——	Hz
Input voltage	H level	VIH	V_{DD}-Vss =5.0V±10%	0.8VDD	——	V_{DD}	V
	L level	VIL		Vss	——	0.2V_{DD}	V
Current Consumption		ISS	Ta=25°C	——	5.6	9.1	mA
			V_{DD}-Vss=5.0V				
			V_{DD}-V_{EE}=17.2V	——	7.9	12.2	mA
		IEE	f_{FRAHE}=70Hz				
		IEL	Ta=20°	——			
			AC100Vrms, 400Hz	——	31	40	mA

* V_{DD} > Vss > VEE

4-3 Operating voltage for LCD driving (VDD-VEE)

The contrast of the liquid crystal display depends on viewing angle, ambient temperature, and operating voltage, etc. Adjust the contrast by varying VEE as necessary.

The following values are recommended.

Ta=32°F (0°C) ..... 18.3 Vtyp ϕ=0°

Ta=77°F (25°C) ..... 17.2 Vtyp θ=0°

Ta=104°F (40°C) ..... 16.2 Vtyp

4-4 V0 adjusting circuit

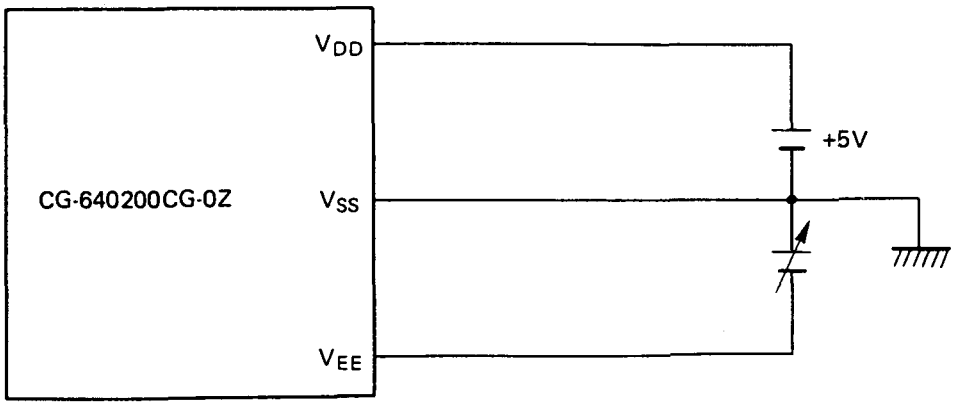


Figure A-3. V0 Adjusting Circuit

5. Interface Specifications

5-1 Terminal Pin Assignment

Pin No.	Symbol	Function
1-4	UD0-UD3	DATA input signal of upper screen (Fig A-4)
5-8	LD0-LD3	DATA input signal of lower screen (Fig A-4)
9	V_{SS}	GND
10	CP	Shift register clock pulse for segment driver.
11	LOAD	Signal for latching 1 line shift register DATA & common driver DATA shift signal.
12	DF	A.C. signal for LCD driving
13	FRAME	Start signal of each display cycle (Shift register DATA signal of common driver)
14	NC	No connection
15	V_{DD}	+5V (Supply voltage for logic circuit)
16	V_{SS}	GND
17	V_{EE}	Supply voltage for LCD driving
18	V_{EL1}	Supply voltage for EL Back light
19	V_{EL2}	Supply voltage for EL Back light (GND)
20	NC	No connection

5-2 Relationships of DATA input signal and LCD Screen division

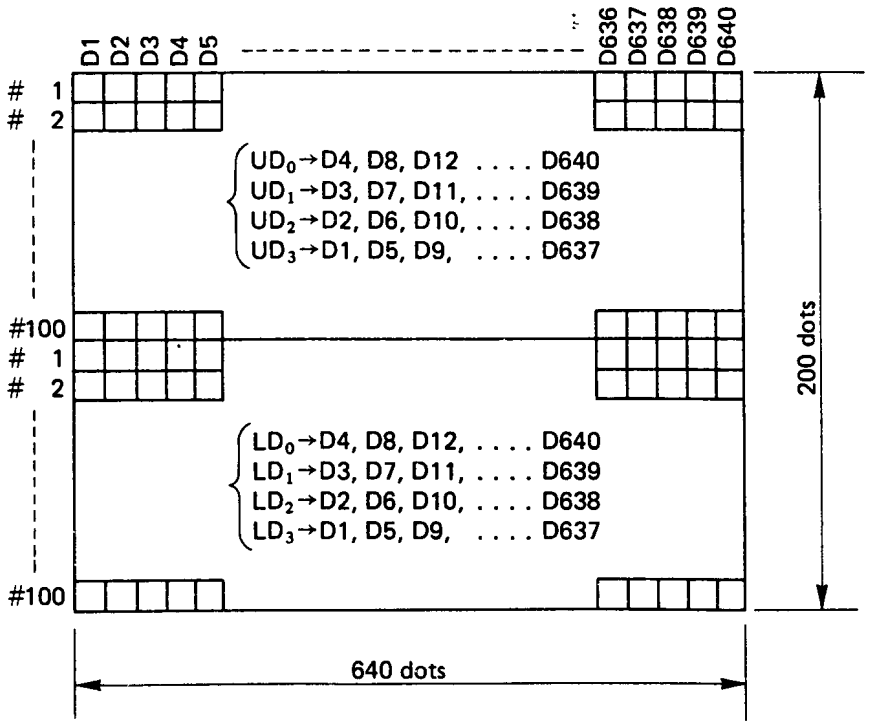


Figure A-4. LCD Sreen

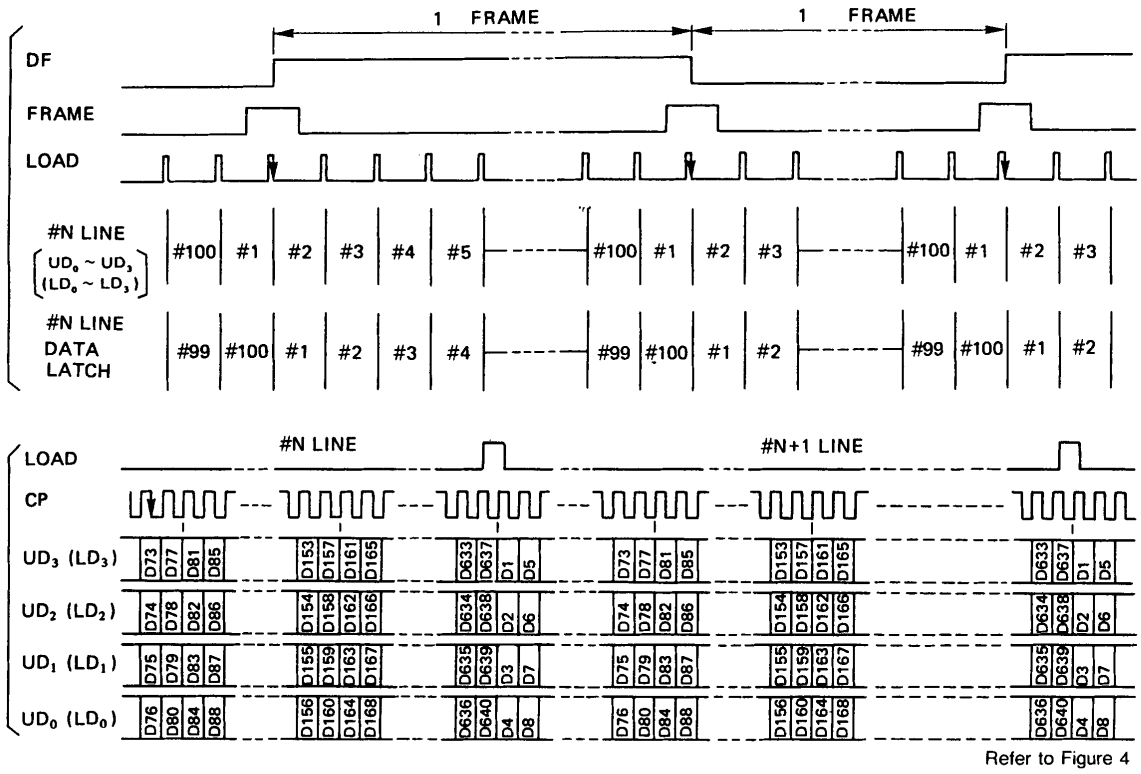


Figure A-5. Timing Chart

5-4. Switching Characteristics

V_{DD} = 5V ± 10%, Cload = 15 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CP frequency	f CP	DUTY=50%	——	——	3	MHz
CP LOAD palse width	t W	——	125	——	——	ns
DATA SET UP TIME $UD_0 \sim UD_3 (LD_0 \sim LD_3) \rightarrow CP$	t DSU	——	100	——	——	ns
LOAD SET UP TIME	t LSU	——	125	——	——	ns
LOAD ← CP TIME	t LC, t CL	——	63	——	——	ns
DATA HOLD TIME CP → $UD_0 \sim UD_3$ ($LD_0 \sim LD_3$)	t DHD	——	100	——	——	ns
LOAD → FRAME TIME	t LF	——	2	——	——	μs
FRAME → LOAD TIME	t FL	——	2	——	——	ns
FRAME SET UP TIME FRAME → LOAD	T SETUP (FR)	——	100	——	——	μs
FRAME HOLD TIME LOAD → FRAME	t hold (FR)	——	100	——	——	ns
LOAD → DF DELAY TIME	t LD	——	——	——	300	ns
CR RISE & FALL TIME	t r(CP) t f(CP)	——	——	——	50	ns
LOAD RISE & FALL TIME	t r(L) t f(L)	——	——	——	50	ns
DF RISE & FALL TIME	t r(DF) t f(DF)	——	——	——	100	ns

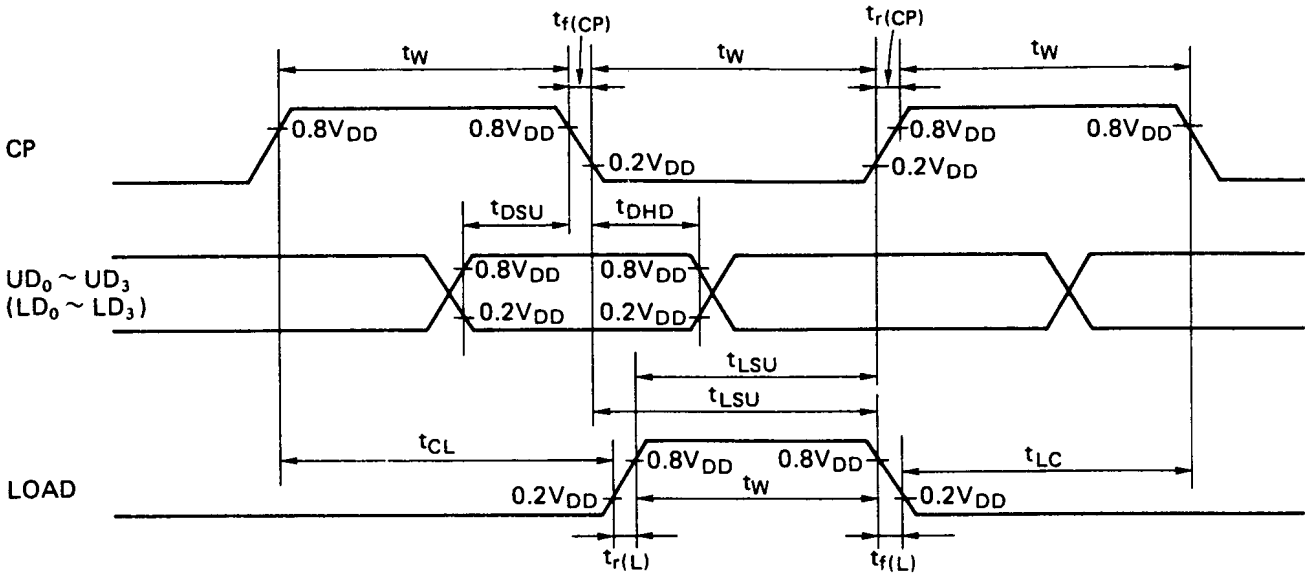


Figure A-6. Timing Chart

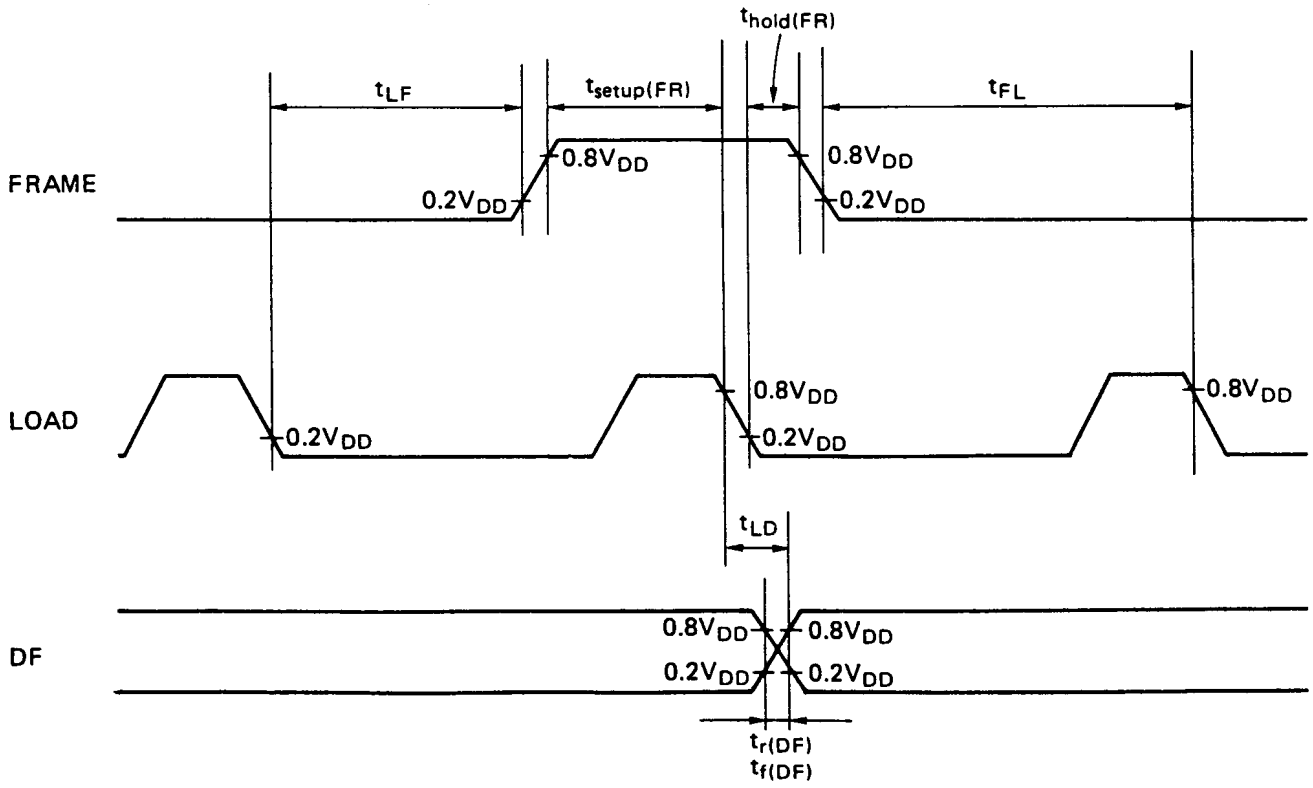


Figure A-7. Timing Chart

6. Optical Characteristics (Refer to Note 1-Note 4)

Ta=25°

Item	Symbol	Minimum	Typical	Maximum	Unit	Condition
Turn on time	tON	——	100	180	ms	$\phi=0°$, $\theta=0°$
Turn off time	tOFF	——	130	230	ms	
Contrast ratio	C	——	5	——		$\phi=0°$, $\theta=0°$
Visual angle range	$\phi 1$	$-35 \leqq \phi^1, \leqq +35$			deg.	$\theta=0°$, C≧1.4
	$\phi 2$	$-45 \leqq \phi^2, \leqq +45$			deg.	$\theta=90°$, C≧1.4
Life time		more than 50000			hour	
EL back light Life time			200		hour	AC100V, 400Hz

*NOTE Life is a time which luminescent rate reaches to 1/2 or lower against initial luminescent 34 cd/m² on EL circuit's becomes 1.2 times on higher.

NOTE 1: Optical Characteristics measurement system

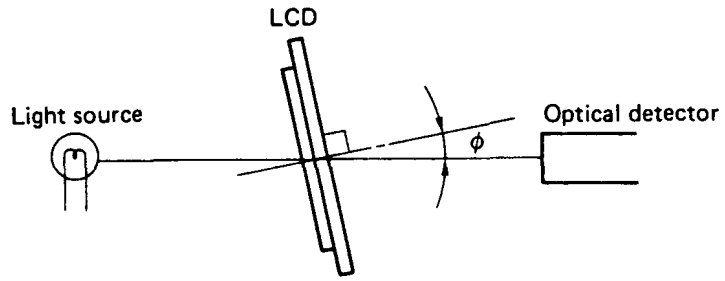


Figure A-8. Optical Characteristics Measurement System

NOTE 2: Definition of response time

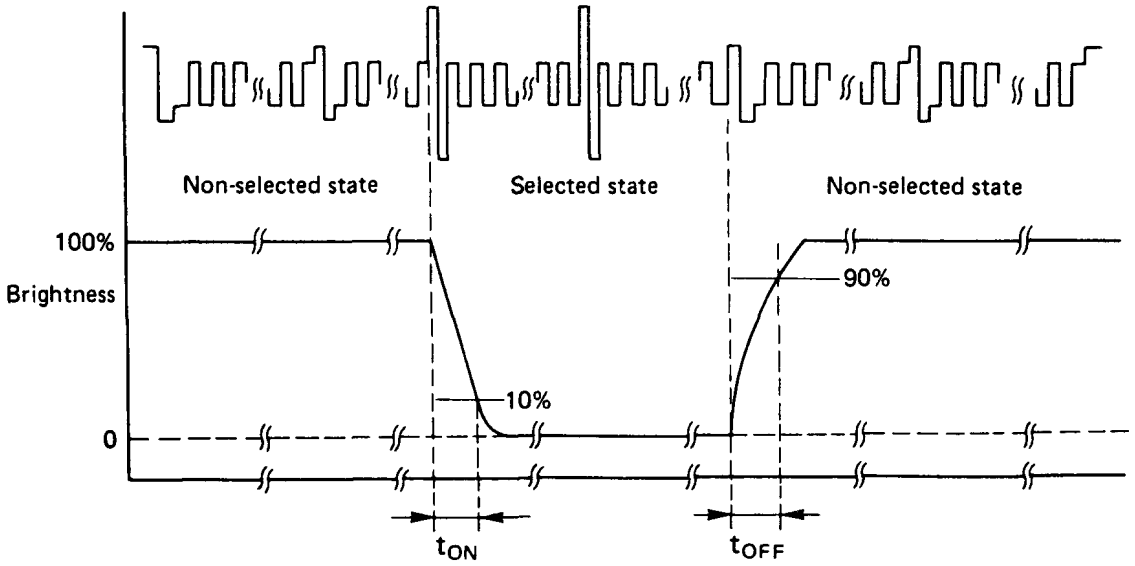


Figure A-9. Definition of Response Time

NOTE 3: Definition of ϕ and θ

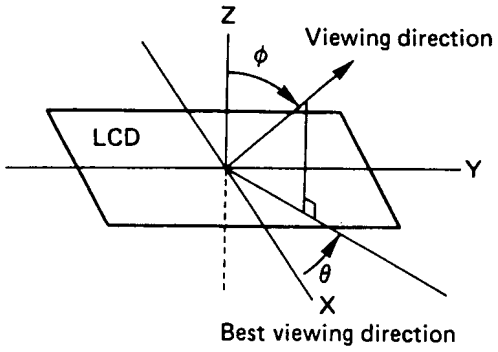


Figure A-10. Definition of ϕ and θ

NOTE 4: Definition of contrast ratio

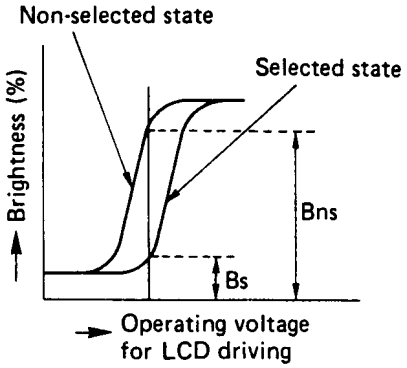


Figure A-11. Definition of Contrast Ratio

$$C = \frac{\text{Brightness at non-selected state (Bns)}}{\text{Brightness at selected state (Bs)}}$$

7. Option

7-1 Pin connector

The product is not provided with any pin connector normally and it is recommended to select one out of the following.

Orders for pin connectors of other makers are acceptable only if the above-noted specifications are met.

	Connectors			Adapting connectors
	Parts name	Standard	Manufacturer	
Option 1	Right angle pin header	UFP-20A-02#2	YAMAICHI	UFS-20A-02
		65532-220	BERG	65039-017
Option 2	Straight pin header	UFP-20A-02#4	YAMAICHI	UFS-20A-02
		66465-220	BERG	65039-017

8. Precautions in use

8-1. Precautions for handling

(1). The polarizer is quite susceptible to scratches. Handle it very carefully. Do not handle it with metallic tweezers nor press nor rub it.

(2). Do not contact the display face by nor get it stained.
If the surface is dirty, wipe it off lightly with a cotton swab or a piece of soft cloth or chamois which is soaked with petroleum or benzine. Never use organic solvents including acetone, toluene, ethanol, and isopropyl alcohol; they would damage the surface.

(3). Do not allow saliva or water to remain on the surface for long; it might cause a local deformation or discoloration.

(4). When the LCD has broken and the liquid crystal has come out, never allow it in your mouth. If it sticks to the skin or clothes, wash it off immediately by using a soap.

8-2. Installation

(1). The ICs mounted on the PCB are very susceptible to static electricity. To protect them from static electricity which your body and clothing collect, connect your body to the ground via a resistor of some 1M ohms so that the electricity should discharge. Connect the resistor close to your body in the grounding line and protect yourself from electric shock hazard.

(2). Neither bend nor twist the module excessively when installing it. Otherwise the device might break or the circuits fail.

(3). Protect the LCD, particularly the surface of polarizer, with a transparent plate (such acrylic or glass plate) on the cabinet.

8-3. Operational precautions

(1). The ICs would break down if the drive voltage exceeds the limit. Make sure of electrical specifications, particularly the supply voltage.

(2). The response of the display is slow when the ambient temperature is below the lower limit, and the display surface appears dark everywhere when the ambient temperature is above the upper limit. In any case, it does not mean failure. It operates properly in the normal operating temperature range.

(3). The contrast of the liquid crystal display varies with the viewing angle, ambient temperature, and drive voltage. Adjust the drive voltage for the best contrast by installing external variable switch.

(4). If you move the module from a cold storage into the room as during test, moisture would condense on the module and it might fail.

(5). In order to prevent IC latch-up and DC voltage on the LCD Panel, please power on by the following Fig. A-12.

8-4. Storage

(1). Avoid high temperature and high humidity. The temperature should be 0-35°C and humidity be under 60%.

(2). Store the module in a dark place, out of direct sunlight and fluorescent lamp, etc.

(3). Keep the polarizer away from any external forces.

(4). Store the module, in the box as it is in delivery or in the same conditions.

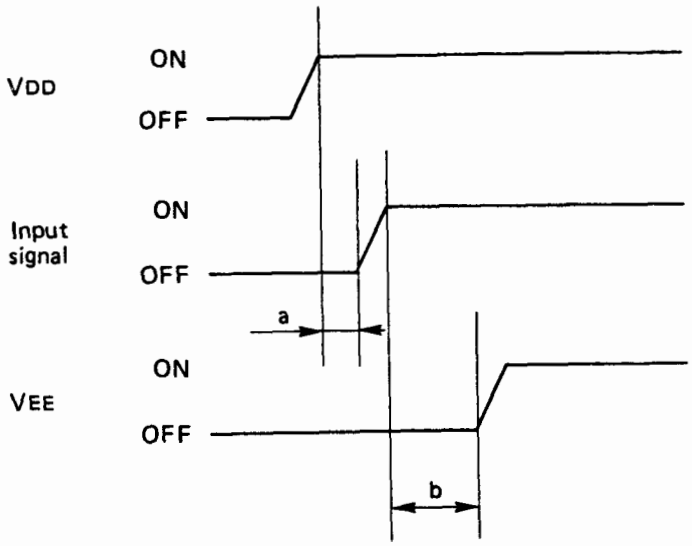


Figure A-12. Operational Precautions

B. REPLACEMENT OF EL BACK LIGHT

EL back light is soldered on two terminals at the right side of the PCB back from the face to the screen.

1. Remove the solders from the two EL back light terminals on the PCB by soldering iron.
   Remark) Be careful not to spread the solder over the other components on the PCB. It may cause shorted. See Fig. B-1.

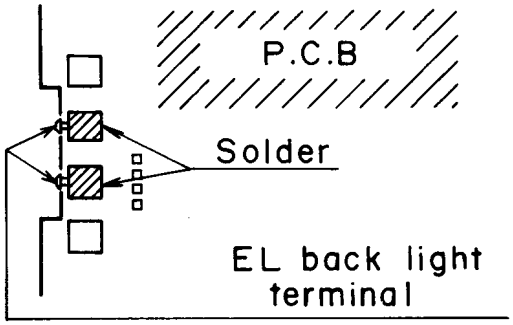


Figure B-1. Unsoldering EL Terminals (Bottom View)

2. Push and remove EL back light from three hooks of the right side of LCD metal frame toward the PCB.
   Remark) Be careful not to scratch the PCB and other components by tools. See Fig. B-2.

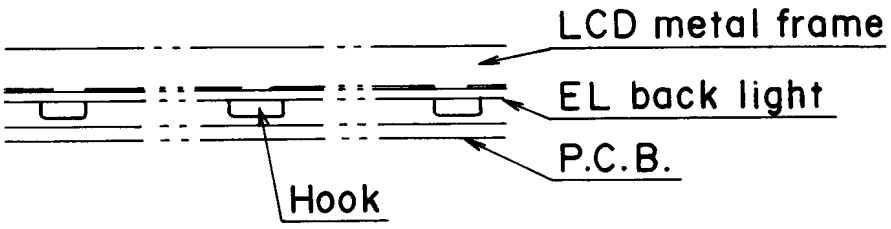


Figure B-2. Detaching EL (Right Side View)

3. Slide and pull out EL back light from the right side. See Fig. B-3.

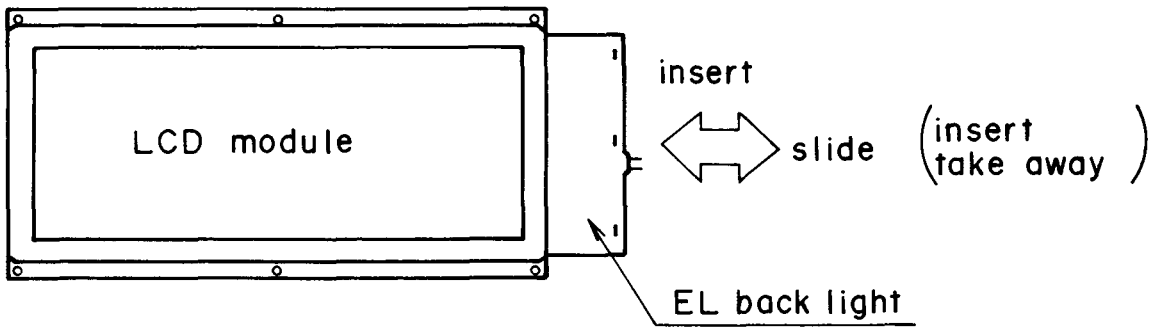


Figure B-3. EL Removal

4. Make sure there are no stain and dust on the replacement EL back light. Clean up by soft cotton cloth or soak benzine lightly and wipe it off when you find out the dust on the surface of the EL back light.
   Remark) If there are dusts on the surface of the EL back light, then you will see some black spot on the screen after lights on the EL.

5. Insert EL back light to original position.
   Remark) There is FPC between left side of module and PCB, so be careful to insert EL back light.
   Bend the head of EL back light lightly upward before insertion.
   And then insert EL back light over the FPC.
   Be careful to watch the silhouette of EL back light when inserting.
   See Fig. B-3 and B-4.
   If you will insert EL back light like as Fig. B-4-a and Fig. B-4-b, it will break the FPC.

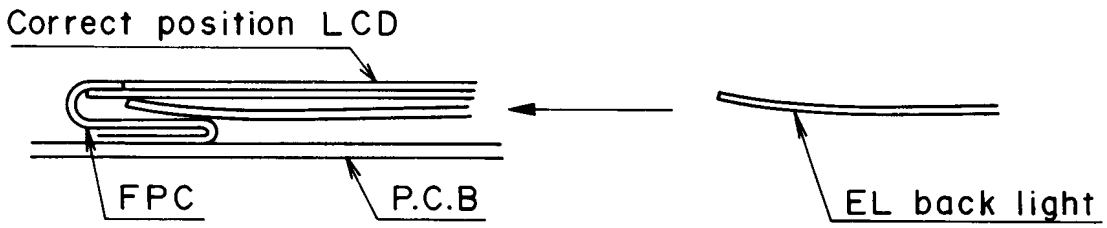


Figure B-4. EL Insertion

Incorrect position

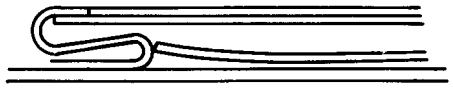


Figure B-4-a. Incorrect Insertion

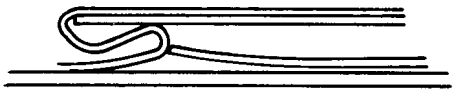


Figure B-4-b. Incorrect Insertion

6. Fit and insert three hooks of the LCD metal frame to the three holes of the EL back light.
   Remark) These hooks are used for fixing the EL back light securely.
   If it is not fixed tightly, then lead wire may get damaged easily. See Fig. B-5.

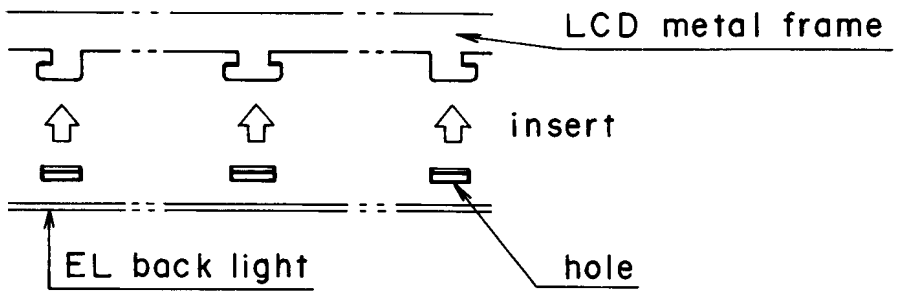


Figure B-5. Attaching EL (Right Side View)

7. Adjust and bend the EL back light terminals to the pad of EL back light terminals, positioned at the back side of the PCB. After that solder them. (EL back light lead wire)
   Remark) Be careful not to give any damage to the component parts when you are soldering. See Fig. B-6.

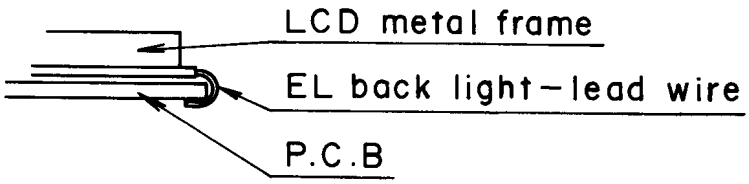


Figure B-6. Soldering EL Terminals

C. 3.5 inch FDD SPECIFICATIONS

1. Introduction

SPECIFICATIONS SUMMARY

Performance Specifications

	Single Density	Double Density
Capacity (Kbytes)		
unformatted		
Per Disk	500	1000
Per Surface	250	500
Per Track	3.125	6.25
Formatted Per Disk		
16 Sectors/Track	327.6	655.2
9 Sectors/Track	368.6	737.2
5 Sectors/Track	409.6	819.2
Transfer Rate (Kbit/sec)	125	250
Average Latency (msec)	100	100
Access Time (msec)		
Track to Track without Settling	6	6
Average with Settling	169	169
Settling Time (msec)	15	15
Motor Start Time (sec)	0.5	0.5

Functional Specifications

	Single Density	Double Density
Rotational Speed (r.p.m)*	300	300
Recording Density (BPI)	4359	8717
Track Density (TPI)	135	135
Tracks	160	160
Encoding Method	FM	MFM

* Rational speed is automatically changed by internal sensor.

Physical Specifications

Environmental Limits	Operating	Shipping	Storage
Ambient Temperature	(5.0° to 45°C)	(−40° to 60°C)	(−20° to 50°)
Relative Humidity	20 to 80%	1 to 95%	1 to 95%
Maximum Wet Bulb	85°F (29.4°C)	no condensation	no condensation

DC Voltage Requirement	+4.4 volt to +5.5 volt
DC Power Current	
Motor start	0.7A Max.
Read	0.31A typ
Write	0.31A typ
Seek	0.85A MAX.
Stand by	0.006A typ
Mechanical Dimensions	
Height	1 inch (25.4 mm)
Width	4 inch (101.6 mm)
Depth	5.9 inch (150 mm)
Weight	1 lb (450 gram)
Shock	
Operating:	3gs with duration of 10 milliseconds
Non-Operating:	60gs with duration of 10 milliseconds

Vibration			
Operating	Frequency	Desplacement	Acceleration
	5-20	0.01 inch	
	20-500		0.5G
Non Operating	5-20	0.27 inch	
	20-100		4.5G

Reliability Specifications

MTBF:	10,000 power on hours under typical usage* * Assumes the duty cycle of the drive spindle motor to be 20%
MTTR:	30 minutes
Component Life:	5 years
Error Rates:	
Soft Read Errors:	1 per 10^9 bits read
Hard Read Errors:	1 per 10^{12} bits read
Seek Errors:	1 per 10^8 seeks
Media Life:	
Passes per Track:	3.0×10^6
Insertions:	20,000 +

FUNCTIONAL CHARACTERISTICS

General Operation

The FDD consists of:

(1) Read/Write and Control Electronics
(2) Drive Mechanism
(3) Precision Track Positioning Mechanism
(4) Read/Write Head (s)

Fig. C-1 shows interface signals for the internal functions of the FDD

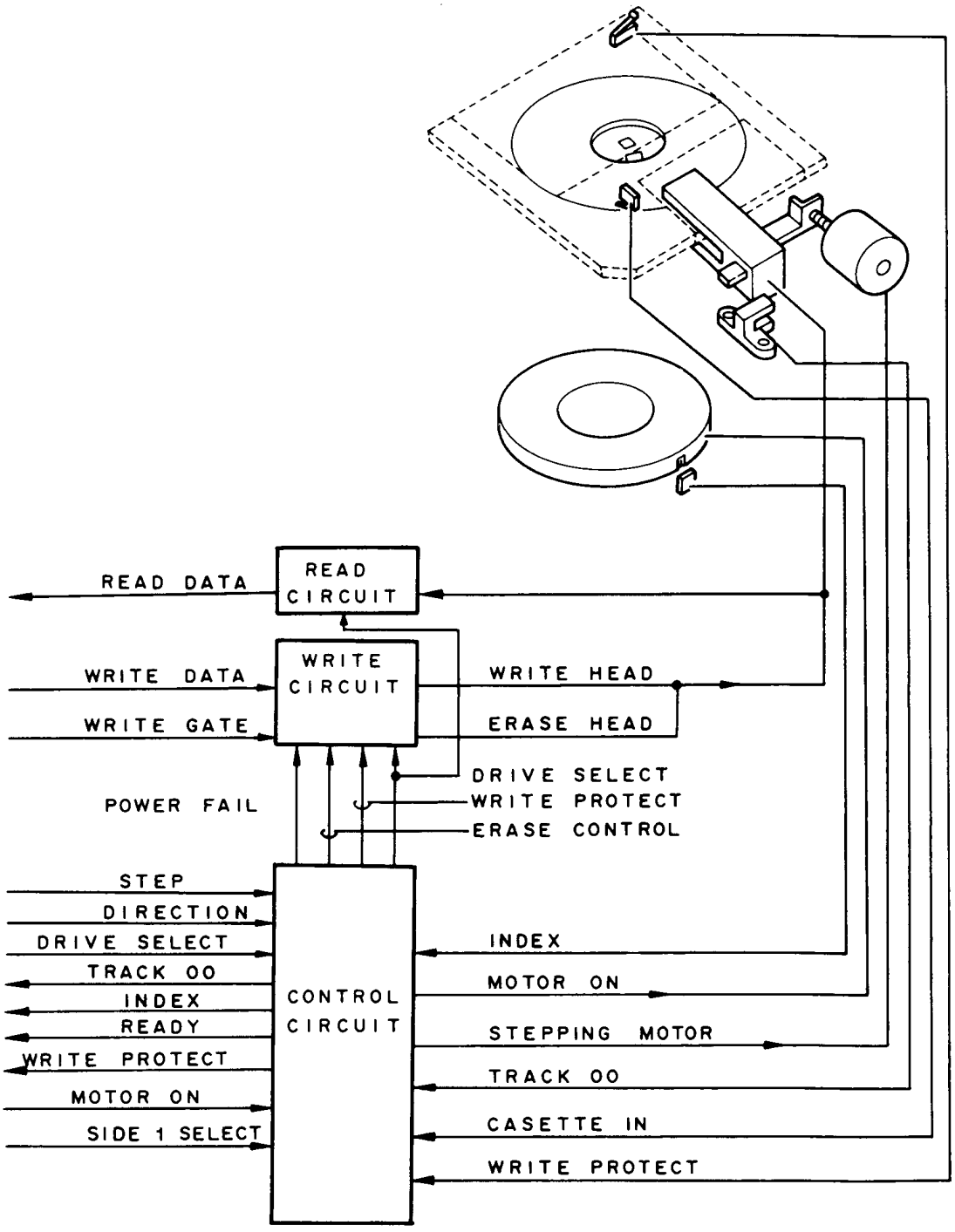


Figure C-1. Functional Diagram

Read/Write and control electronics

The FDD has following components.

(1) Index Circuit
(2) Head Position Actuator Driver
(3) Read/Write Amplifier and Transition Detector
(4) Write Protect Circuit
(5) Drive Select Circuit
(6) Standby Circuit
(7) InUse Lamp Circuit
(8) Voltage Detector
(9) Spindle Motor Start/Stop
(10) Track 00 Circuit
(11) Side 1 Select Circuit

The Head Positioning Actuator moves the read/write heads to the desired track on the disk. The media cartridge is loaded onto the read/write heads by an elevator mechanism with an oil damper when the cartridge is inserted.

Drive Mechanism

The brushless direct drive motor rotates the spindle at 300 rpm. Like conventional 5.25" drives, the FDD has a MOTOR ON signal. Since almost all of the power of the FDD is turned off when the MOTOR ON signal is "High", the power consumption in the standby mode is low.
the motor control circuit is printed on the Stator Yoke (material: iron) of the spindle motor and the Index Pulse is generated by the hall sensor.

Positioning Mechanism

In order to achieve high accuracy in track positioning, the head is positioned by a lead screw mechanism. The stepping motor rotates the lead screw clockwise or counter-clockwise and moves the read/write heads from track to track.
If the heads is positioned at Track 00, Step signal to outer track is rejected.

Disk Chucking Mechanism

The 3.5″ media utilizes a chucking hole which maintains excellent track positioning accuracy without causing eccentricity or chucking wear. (See Fig. C-2)

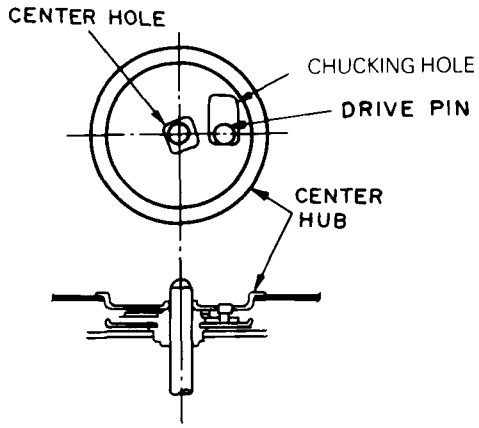


Figure C-2. Disk Chucking Mechanism

Read/Write Heads

The bulk type ferrite read/write heads contain tunnel erase elements to provide erased areas between data tracks.

2. Electrical Interface

INTERFACE CONNECTION

The FDD interface connection is shown in Fig. C-3.

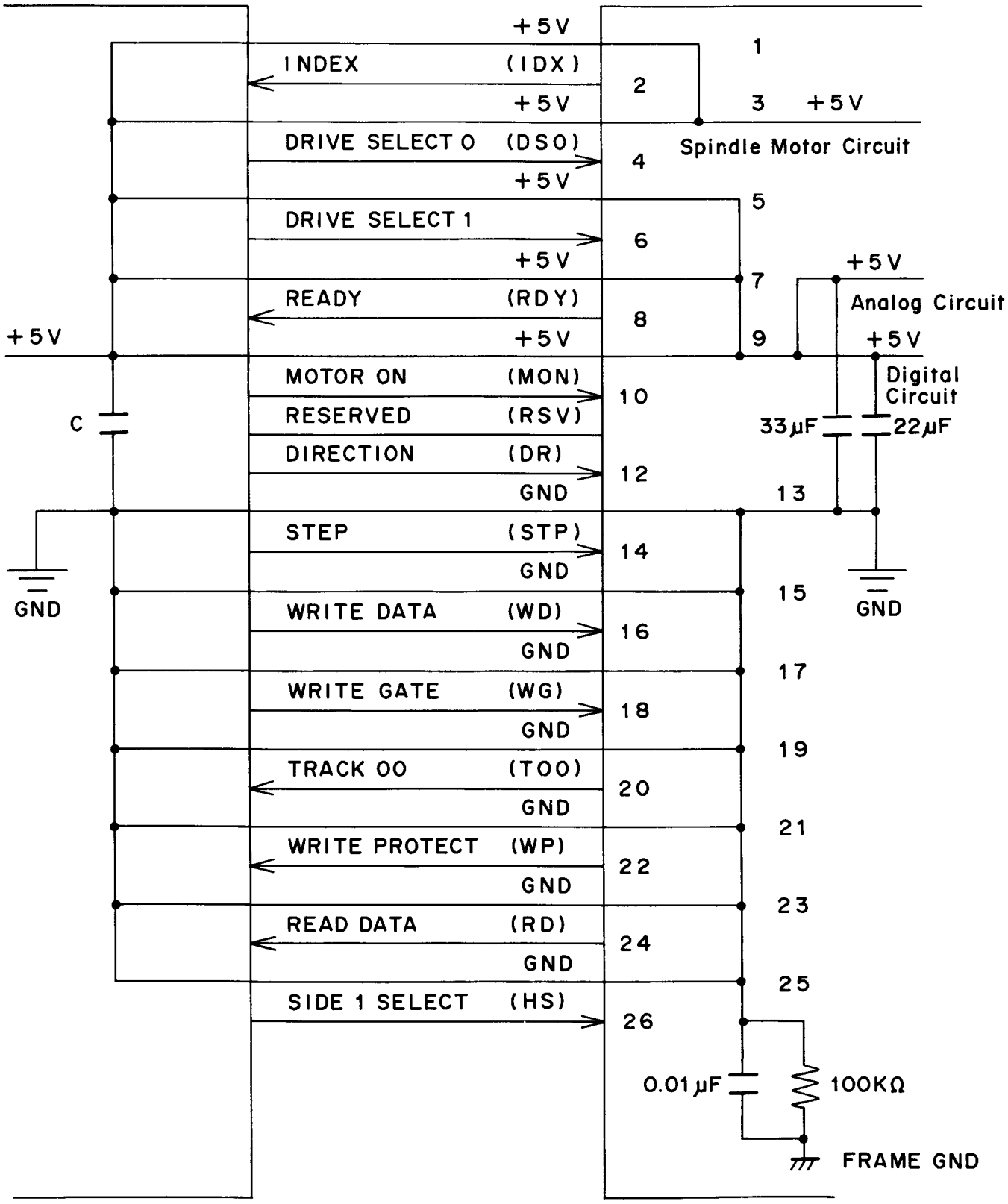


Figure C-3. Interface Connections

INTERFACE CIRCUITS

The FDD uses an open collector as output line drivers, and CMOS as input line receivers. It is recommended that an open collector (SN7438, 06, 07 or equivalent) should be used as output drive of the controller side and SN74LS14 or equivalent as input receiver. Each input receivers is terminated in 10kΩ to Vcc.

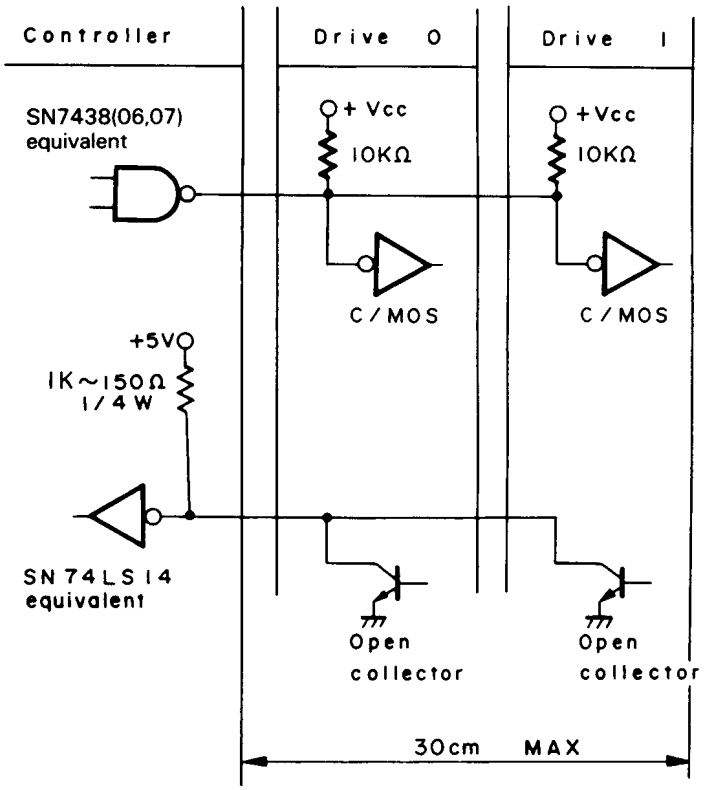


Figure C-4. Recommended Circuit

INTERFACE SIGNALS

Interface signals have the following characteristics.

Input Signals	
"High" Level	3.0 to Vcc
"Low" Level	0 to 0.8V
Input Impedance	1kΩ terminated to Vcc
Output Signals	
"High Level	Source Current: 100μA max.
"Low" level	0.6V max.
	Sink Current = 40 mA

Table C-1. Input and Output Level

INPUT SIGNALS

The FDD has the following input lines.

(1) DRIVE SELECT 0 TO 1
(2) MOTOR ON
(3) DIRECTION
(4) STEP
(5) WRITE DATA
(6) WRITE GATE
(7) SIDE 1 SELECT

DRIVE SELECT 0 TO 1

Two input lines are provided for drive select, DRIVE SELECT 0 TO 1.
Up to two drives can be daisy chained by setting the drive select switch on the PCB.
A "Low" level on input signal DRIVE SELECT 0 enables the drive to operate when the drive select switch is set to "DS0".
The other drives in the chain can be selected in the same way.
The setting position on the select switch must be different for each drive in the chain.

MOTOR ON

The Spindle Motor starts when this signal becomes "Low".

DIRECTION

This signal determines the direction of R/W Heads movement by the following:
"High" Level: Out (towards Track 00)
"Low" Level: In (towards Track 79)

STEP

This line causes the R/W Heads to move.
The period of a STEP pulse must be a minimum of 6ms.
A (21 ms) delay following the last STEP pulse is required before the read or write operation can be initiated.
A (21 ms) delay following the last STEP pulse is required for the next STEP pulse when the DIRECTION is changed.
The following examples describe several cases that make STEP pulses valid or invalid.
(1) STEP pulses towards the outside after the TRACK 00 signal has been generated are invalid.
(2) STEP pulses whose intervals are less than 6 ms may cause seek errors.
(3) A STEP pulse should be generated at more than 21 msec. when DIRECTION signal has been reversed.

Fig. C-5 shows step pulse timing.

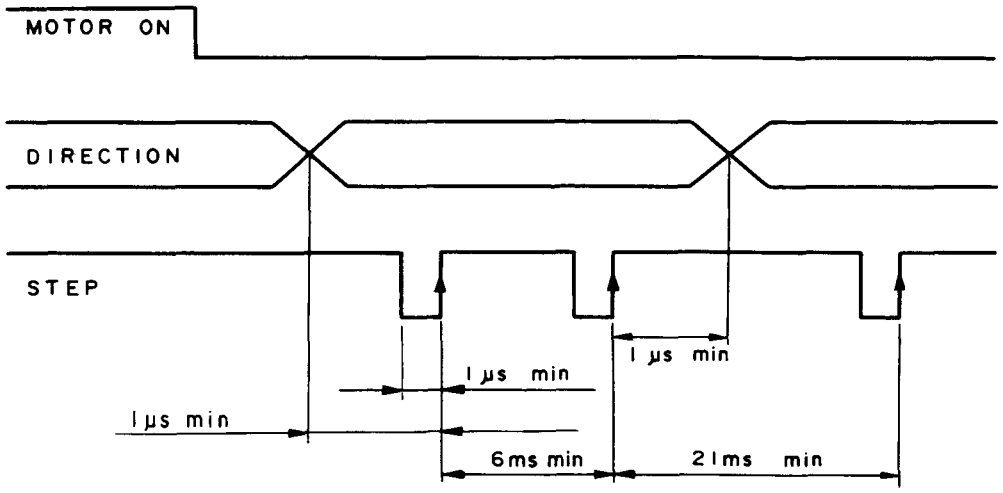


Figure C-5. Step Pulse Timing

In consideration of a delay of a STEP pulse in a drive, the DIRECTION is latched at the trailing edge of the STEP pulse.

Write Data

This line provides data to be written on the disk.

Each transition from "High" to "Low" changes the polarity of the R/W Head Current and causes a data bit to be written on the disk.

Figure C-6 illustrates the Write Data timing in MFM recording.

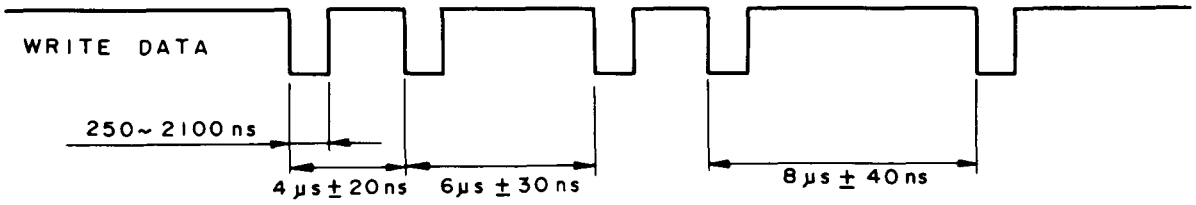


Figure C-6. Write Data Timing (MFM)

When the power turned on or when the source voltage is suddenly dropped lower than 3.5V and returned to the normal voltage, the write data signal is invalid for 10 msec after the source voltage returns to a normal level.

Write Gate

A "Low" level on this line enables writing.

When the READ DATA or STEP lines are activated, the signal on this line must be "High". The change of DRIVE SELECT, start of reading, and STEP must be delayed 1.5 ms after WRITE GATE becomes "High", because the erase head is operated for this time. When the above is not observed, it may cause a data error.

Figure C-7 illustrates the timing for WRITE GATE and WRITE DATA.

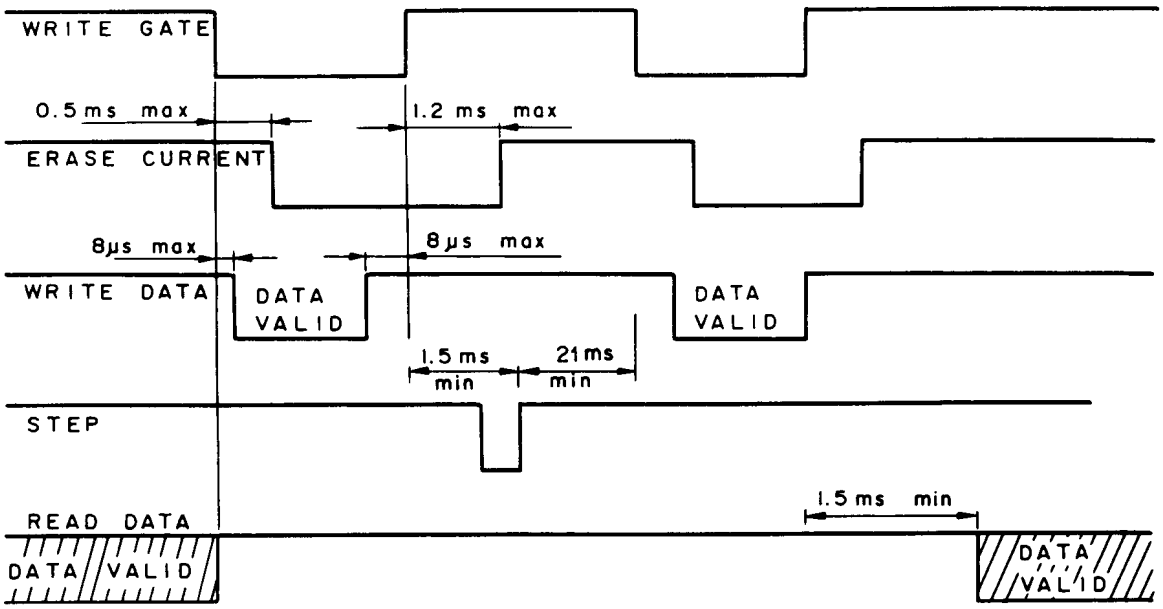


Figure C-7. Write Gate and Write Data Timing

Side 1 Select

A "Low" level on this line selects side 1 and "High" selects side 0.

When the WRITE GATE is "Low", the change of a side is invalid.

Output Signals

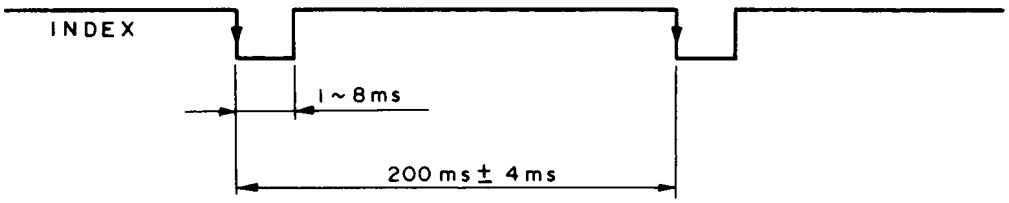
Output signals are as follows:

(1) INDEX
(2) TRACK 00
(3) WRITE PROTECT
(4) READ DATA
(5) READY

Index

This line is used for indicating the reference position of a track.
The leading edge of an Index pulse should be used when an Index signal is needed.

Figure C-8 shows the Index signal timing.



The wow-flutter is ± 1.5% max.

Figure C-8. Index Signal Timing

Track 00

This signal becomes "Low" when the R/W Heads is positioned at track 00.
Fig. C-9 shows the timing for the last STEP pulse and the TRACK 00 signal.

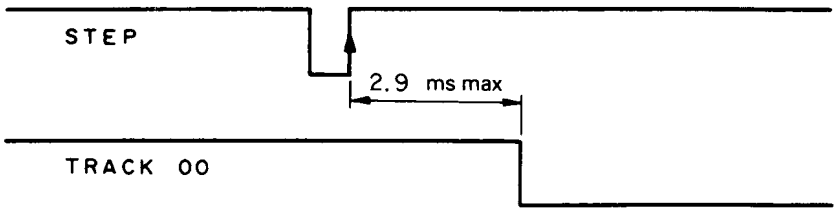


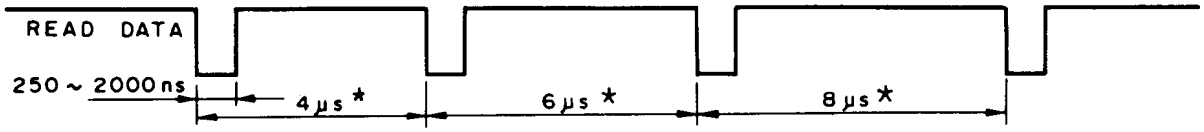
Figure C-9. Track 00 Signal Timing

Write Protect

A "low" level on this line indicates that the disk inserted in the drive is write-protected, or the Vcc is below the level for write protect.

Read Data

This line provides "raw data" (clock and data information unseparated). See the Figure C-10.



Note: 1) Figures with * indicate the nominal positions.
2) The accuracy of READ DATA to reference position is within ± 0.7 µs

Figure C-10. Read Data Timing

READY

A "Low" level on this line indicates that the drive is ready.

The READY signal becomes "Low" when all of the following conditions are satisfied.

(1) The drive is selected.

(2) A cartridge is correctly loaded.

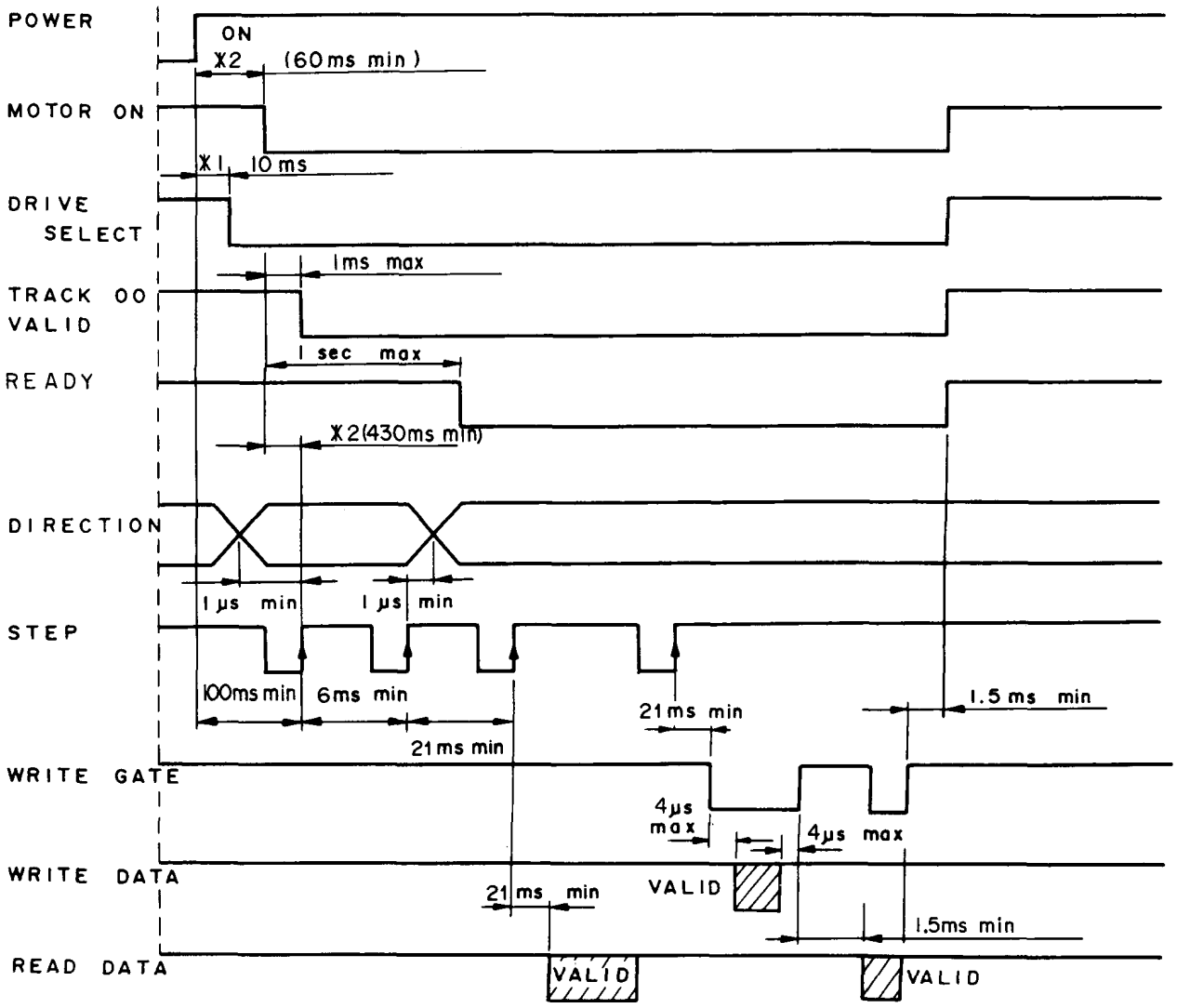
(3) Vcc is 4.2V min.

(4) Two INDEX pulses are generated after the INDEX cycle is fixed.

The READY signal becomes "Low", a maximum of 1 sec after the Spindle Motor starts to run.

INTERFACE TIMING

Figure C-11 shows the timing relationship for Host/Drive interface signals.



*1 All input/output signals are off for 100 ms from Power On because of internal protect function.

*2 ( ) is our recommended value to keep power consumption small.

Figure C-11. Timing Relationship for Host/Drive Interface Signal

POWER INTERFACE

The power supply and current are shown in Table C-2.

	Current (mA)					
	4.4V		5V		5.5V	
	TYP	MAX	TYP	MAX	TYP	MAX
Standby	5.6	(6)	6.5	(7)	7.0	(8)
Read/Write	280	340	300	360	320	380
Seek * (AVE.)	440	500	490	550	530	590
Motor Start *2	710	750	750	790	780	870

(Seek: 6 msec track to track)

*1: Spindle Motor on.
*2: For about 100 msec from Motor on.

Table C-2. Power Supply and Current

OTHER FUNCTIONAL CHARACTERISTICS

Automatic Motor On/Off

The Spindle Motor starts when both of the following conditions are satisfied.

a) The cartridge is correctly loaded.
b) The MOTOR ON signal is "Low".

The Sindle Motor stops when either of the above is not satisfied.
Figure C-12 shows the timing of the spindle motor rotation.

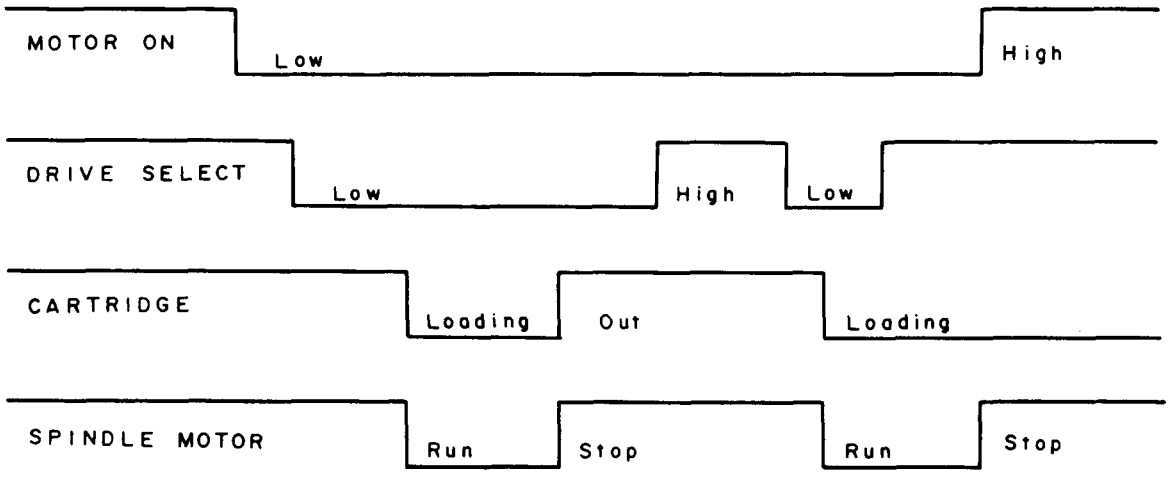


Figure C-12. Timing of the Spindle Motor Rotation

Standby
When the Motor On Signal becomes "High", the power consumption is very little in the standby mode.

Vcc Detector.
The FDD has a Vcc detector in itself.

Figure C-13 shows the operation of Vcc detector.

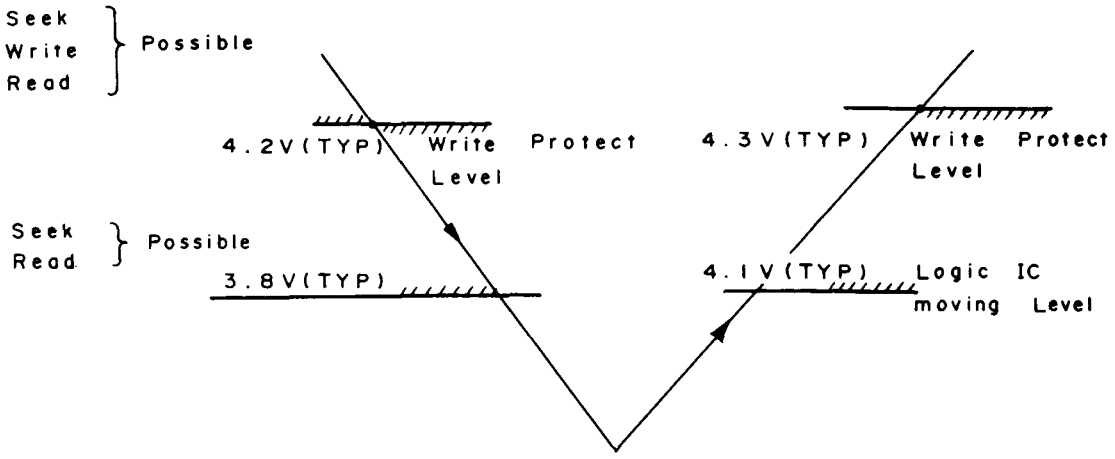


Figure C-13. Vcc Detector

In Use Lamp
In Use Lamp lights when cartridge is incerted, and both DRIVE SELECT and MOTOR ON signals are low.

3. Physical Interface

CABLE CONNECTIONS

The electrical interface between the FDD and the host system is via two connectors. The first connector, CN-1, provides the signal interface, and the second connector, CN-2, provides the DC power. Figure C-14 shows the diagram of cable connections.

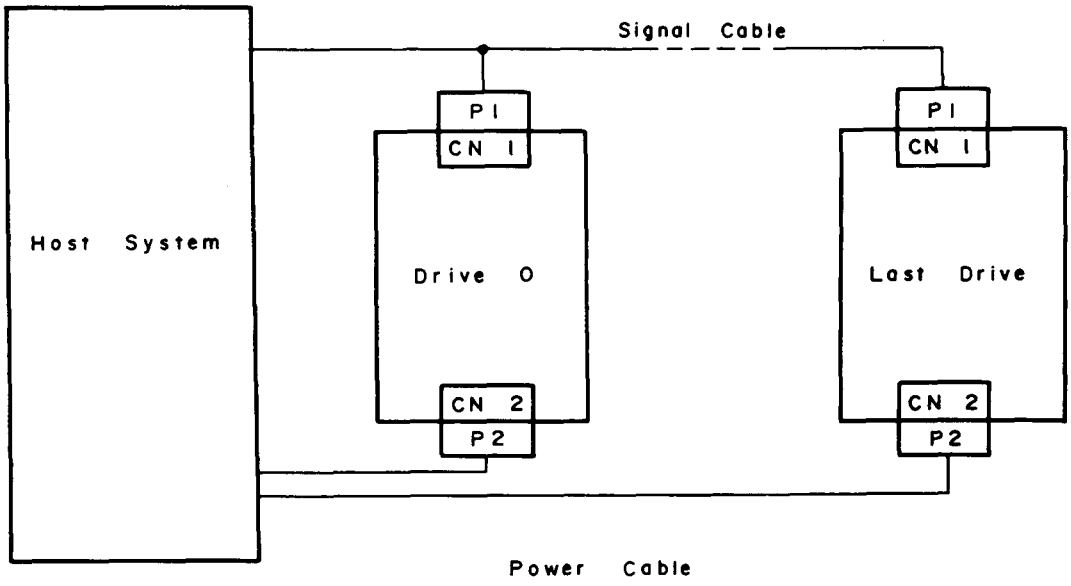


Figure C-14. Cable Connections

Table C-3 shows the signal connector pin assignments.

Pin No.	Signal	Pin No.	Signal
1	Vcc for SP MOTOR	2	INDEX
3	Vcc for SP MOTOR	4	DRIVE SELECT 0
5	Vcc for Analog circuit	6	DRIVE SELECT 1
7	Fcc for Analog circuit	8	READY
9	Vcc for Analog circuit	10	MOTOR ON
11	RESERVED	12	DIRECTION
13	RETURN	14	STOP
15	RETURN	16	WRITE DATA
17	RETURN	18	WRITE GATE
19	RETURN	20	TRACK 00
21	RETURN	22	WRITE PROTECT
23	RETURN	24	READ DATA
25	RETURN	26	SIDE 1 SELECT

Table C-3. Signal Connector Pin Assignments

4. Installation

MECHANICAL DIMENSION

The mechanical dimensions of 0PDB-12A are as follows:

Width: 4.00 ± 0.02 inches (101.6 ± 0.5 mm)
Depth: 5.91 ± 0.02 inches (150.0 ± 0.5 mm)
Height: 1.00 ± 0.02 inches (25.4 ± 0.5 mm)

Figure C-15 shows the dimensions

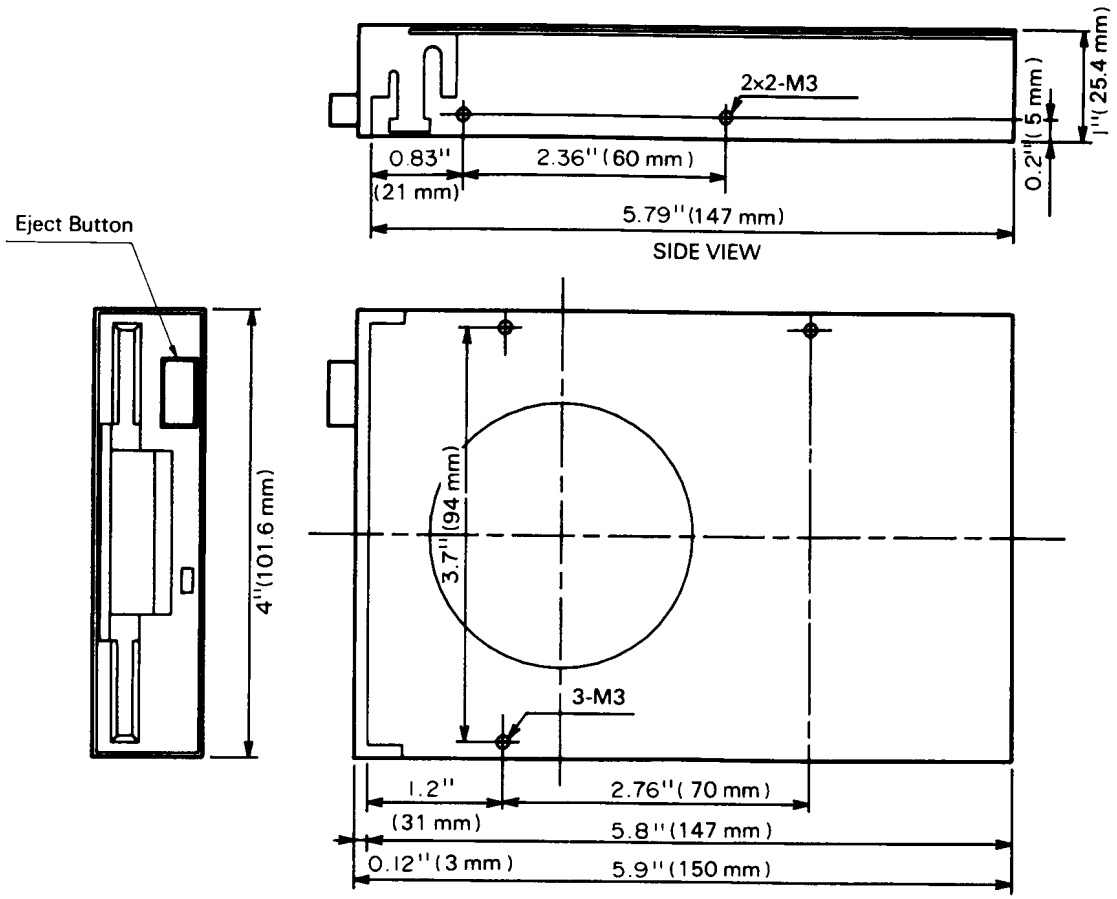


Figure C-15. Mechanical Dimensions

MOUNTING DIRECTIONS

The FDD can be mounted in three ways as shown in Figure C-16.

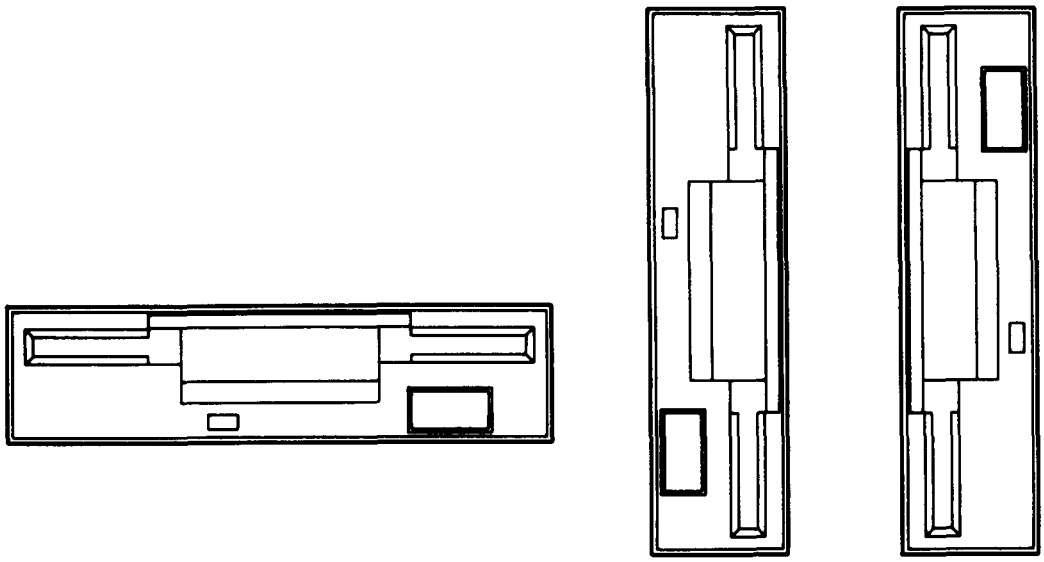


Figure C-16. Recommended Mounting Direction

If the drive is mounted at an angle should not exceed 30 degrees. (See Figure C-16)

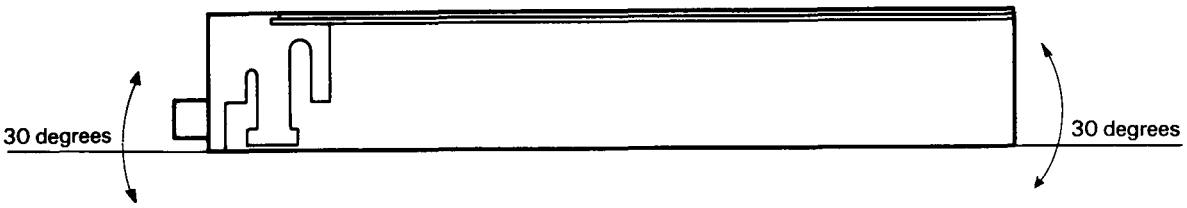


Figure C-17. Mounting Angle

5. Operation Procedure

DISK LOADING/EJECTING

Insert the disk into the drives with "Label" on PCB side as shown in figure C-18.
When unloading the disk, push the Eject Button on the front bezel. (See Figure C-15)

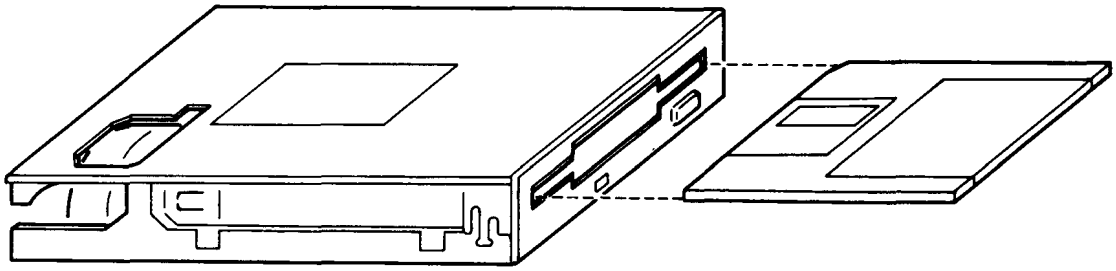


Figure C-18. Cartridge Loading

DRIVE SELECT CONTROLS

The Drive Select switch located at the left side of the FDD is used to designate drives 0 up to 1 in a daisy chain application. The FDD is shipped from the factory designated as a drive 0. If the drive is designated other than drive 0, set the Drive Select switch to the applicable position.

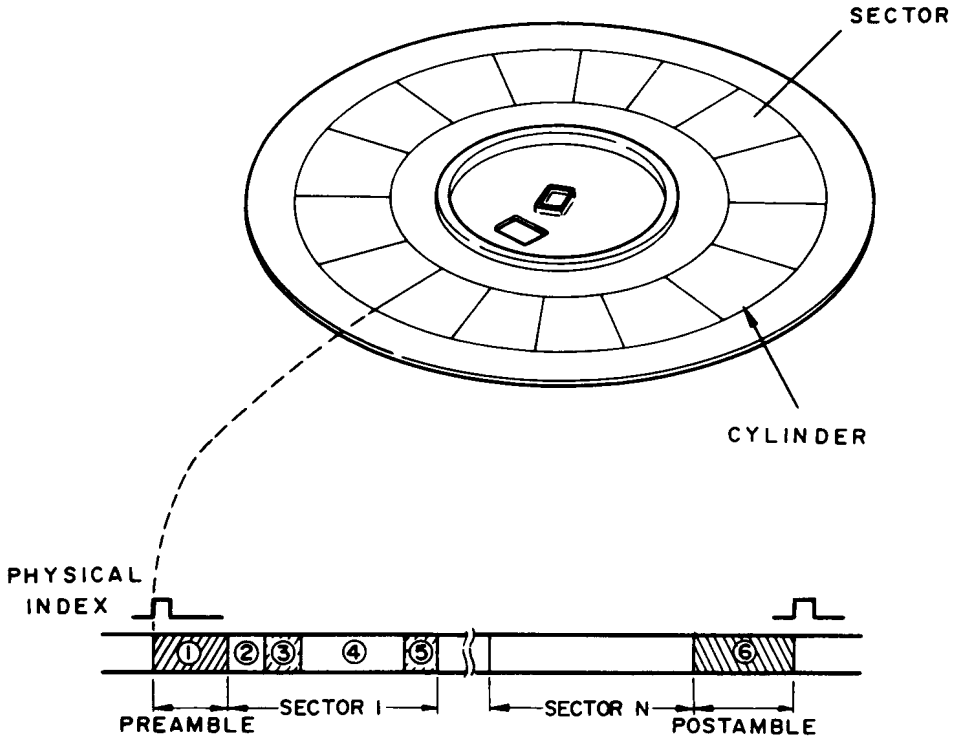
6. Recording Format

RECORDING FORMAT

The format of the data recorded on the disk is totally a function of the host system, and can be designed around the user's application to take best advantage of the total available bits that can be written on any track.
Table C-4, Fig. C-19, C-20, and Fig. C-21 show the typical recommended format.

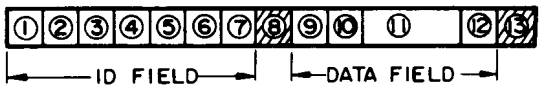
	IBM FORMAT	Tandy FORMAT
128/256 Bytes/Sector	15 Sectors (FM)	16 Sectors
256/512 Bytes/Sector	9 Sectors	9 Sectors
512/1024 Bytes/Sector	4 Sectors	5 Sectors

Table C-4. Recommended 1MB Format



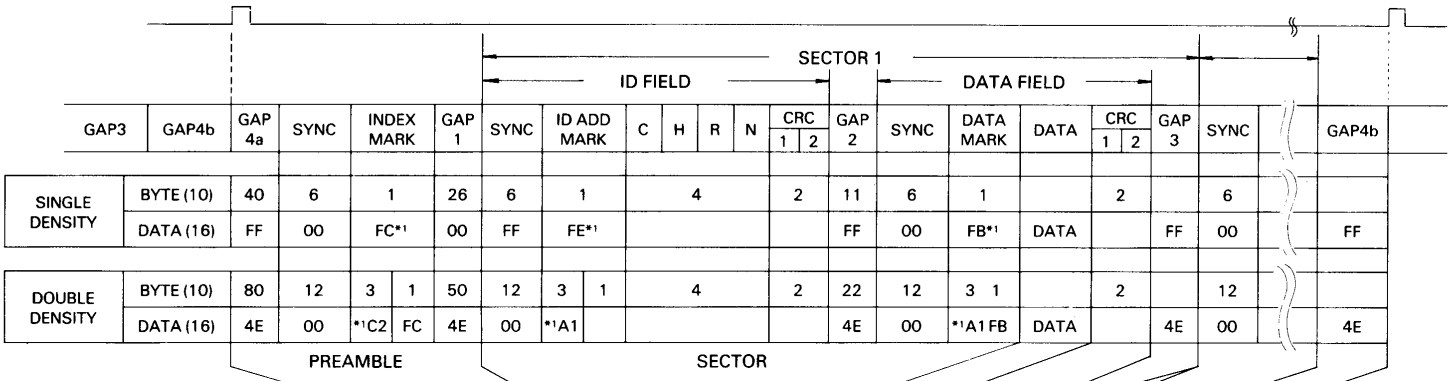
① GAP 1
② ID FIELD
③ GAP 2
④ DATA FIELD
⑤ GAP 3
⑥ GAP 4

SECTOR FORMAT



① SYNC
② ID ADDRESS MARK
③ CYLINDER NUMBER
④ HEAD NUMBER
⑤ RECORD NUMBER
⑥ RECORD LENGTH
⑦ CRC
⑧ GAP2
⑨ SYNC
⑩ DATA ADDRESS MARK
⑪ DATA
⑫ CRC
⑬ GAP 3

Figure C-19. Allocation of the Track Format

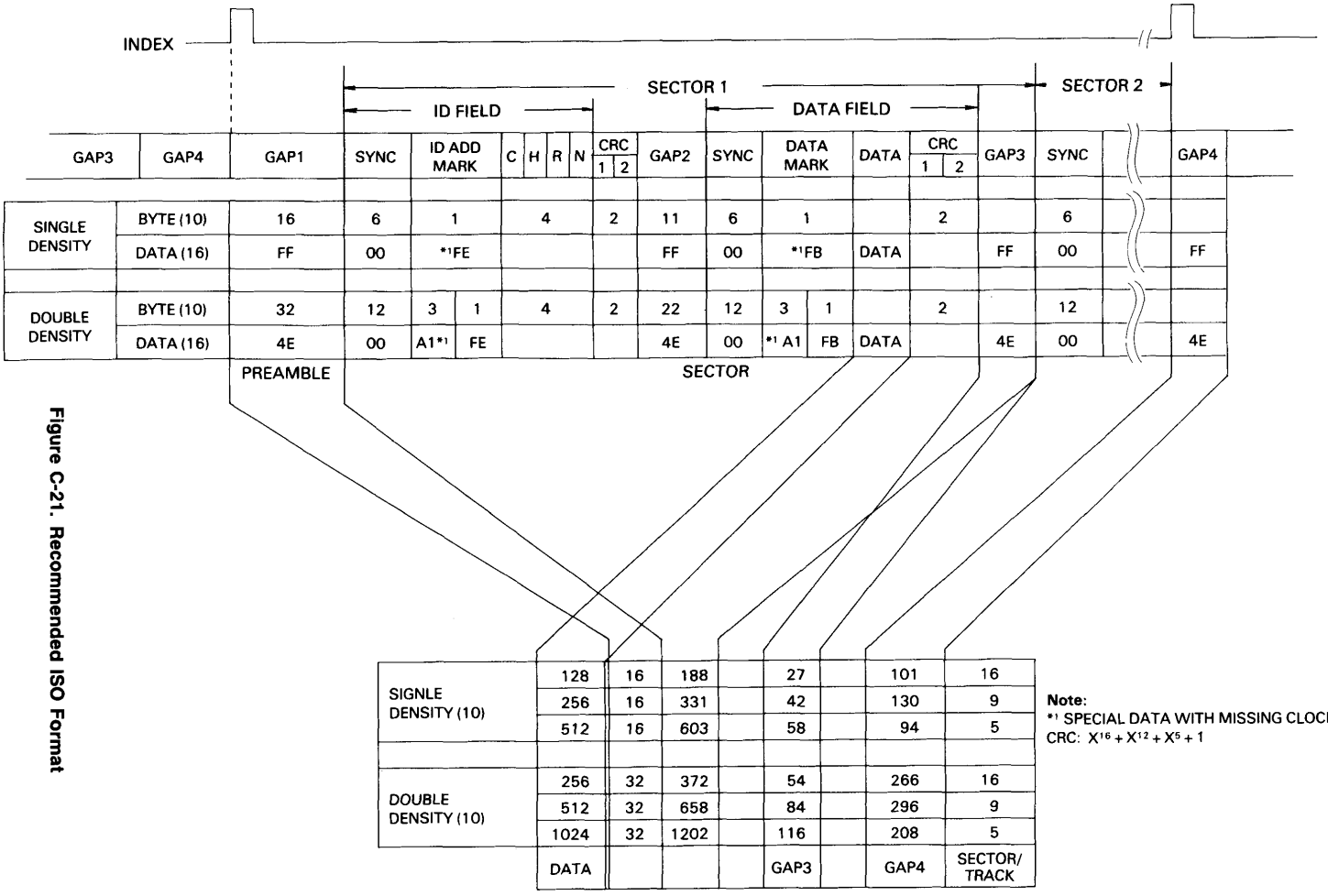


SIGNLE DENSITY (10)	128	73	188	27	232	15
	256	73	331	42	73	9
	512	73	603	58	640	4
DOUBLE DENSITY (10)	256	146	372	54	524	15
	512	146	658	84	182	9
	1024	146	1202	116	1296	4
	DATA			GAP3	GAP4	SECTOR/ TRACK

Note:
*1 SPECIAL DATA WITH MISSING CLOCK
CRC: $X^{16} + X^{12} + X^5 + 1$

	SINGLE DENSITY		DOUBLE DENSITY	
	DATA	CLOCK	DATA	CLOCK
INDEX ADDRESS MARK	FC	D7	FC	01
ID ADDRESS MARK	FE	C7	A1, FE	0A, 00
DATA ADDRESS MARK	FB	C7	FB	00
DELETED DATA ADDRESS MARK	F8	C7	F8	03
GAP	FF	FF	4E	90
SYNC	00	FF	00	FF
INDEX MARK	–	–	C2	14
ADDRESS MARK	–	–	A1	0A

Figure C-20. Recommended IBM Format



SIGNLE DENSITY (10)	128	16	188		27	101	16
	256	16	331		42	130	9
	512	16	603		58	94	5
DOUBLE DENSITY (10)	256	32	372		54	266	16
	512	32	658		84	296	9
	1024	32	1202		116	208	5
	DATA			GAP3		GAP4	SECTOR/ TRACK

Note:
*1 SPECIAL DATA WITH MISSING CLOCK
CRC: $X^{16} + X^{12} + X^5 + 1$

Figure C-21. Recommended ISO Format

D. 3.5 inch FDD MAINTENANCE

1. Tools and Measuring Instruments

1-1 GENERAL AND SPECIAL TOOL LIST

The tools and measuring instruments for performing maintenance.

a) General Tools
   Screw Driver Set
   Tweezers

b) Special Tools
   FDD TESTER FTS-1
   FDD TEST SYSTEM (Ex. Computer System)

c) Measuring Equipment
   Oscilloscope Dual Trace 20MHz
   Universal Counter

d) Disks
   Standard Disk
   Read/Write Disk (recommend SONY and MAXELL disk)

e) Test Pin
   CST-1-1 (This pin is put into the hall of test point for measurement of test signal.)

2. Trouble Shooting

2-1 BEFORE TROUBLE SHOOTING

The following procedures are recommended to see if the drive is really faulty or not.

1) Incorrect operational procedure.
2) Program error of host system.
3) Poor connection with host system (e.g. GND-related connection, frame GND, etc.).
4) Defective disk; Check that same trouble occurs with other disks.
5) Environmental conditions (where electrical noise easily jumps into signal).
6) Influence of strong magnetic field.
7) Wrong supply voltage.

2-2 TYPES OF ERROR ON A SYSTEM LEVEL

2-2-1 Software Error

Software errors are caused by

1) Dirty heads.
2) Electrical noise.
3) Tracking error.
4) Poor connection with system (GND-related connection).
5) Incorrect motor speed.
6) Incorrect head compliance.

Clean the heads first. Check for index pulse interval and then read error spot more than several times.
If not readable, confirm the heads alignment.
If alignment is wrong, adjust it and read again.
If still not readable, the error is not recoverable.

2-2-2 Write Error

To determine whether the disk or the drive is failing, the disk should be replaced by Read/Write Disk and check that there still exists write error.

If write error does not exist any more, remove the old one.

If write error exists with use of any disk, drive might cause write error.

2-2-3 Seek Eerror

Seek error comes from:

1) Heads movement is incorrect because electrical noise jumps into signal.
2) Heads driving system might be at fault.
   If it is not re-readable after recalibration, drive might be at fault.

2-2-4 Interchange Error

If data written on one drive is readable correctly on another drive, but not by other drives, interchange error exists.

Interchange errors are caused by:

1) Heads are not properly positioned.
2) Motor speed is not correct.
3) Optimum head output level and offset and head compliance are not obtained.
4) Chucking mechanism does not work.

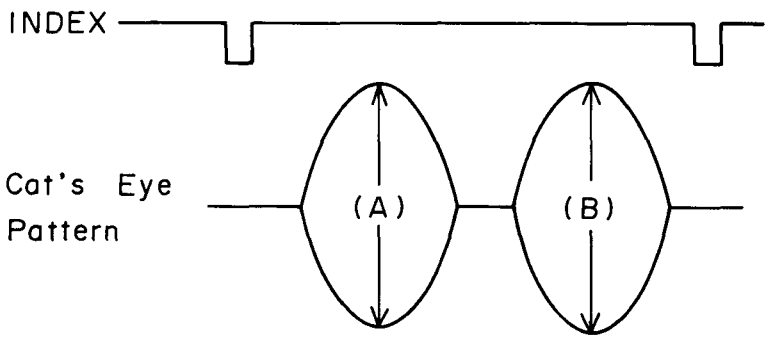
2-3 FAULT DIAGNOSIS BY FDD TESTER FTS-1

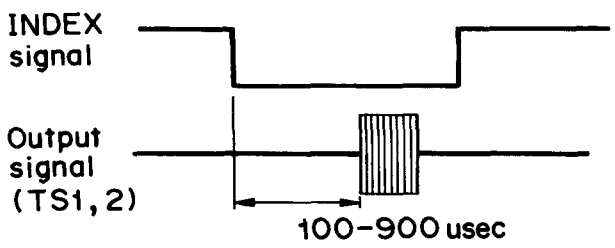
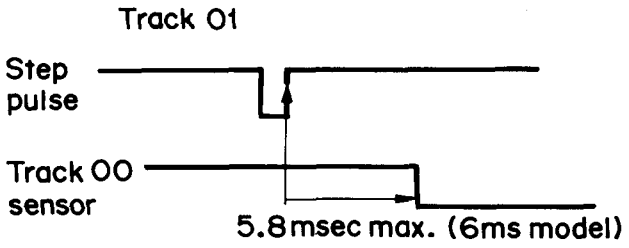
2-3-1 describes check method for normal operation in accordance with the predetermined procedures.
2-3-2 describes check points for abnormal operations which come out in accordance with the above procedures.

2-3-1 Normal Operation

Pre-setting:

1) Refering to operation manual of FDD Tester FTS-1, connect the drive to FTS-1.
2) Set the drive select switch to "0".
3) Set the all the switches of FTS-1 to "OFF".
4) Set the disk in the drive which is not write protected.

1. Power on and push "Reset" button	1. The heads return to Track 00 and stop there. 2. The Track 00 indicator lights.
2. "MOTOR ON" switch on.	1. The spindle motor rotates (See the INDEX signal with oscilloscope) 2. READY indicator lights in about 0.5 seconds after switch is on.
3. Eject the disk	1. The spindle motor stops rotating. 2. READY indicator does not light.
4. Load the disk	1. The spindle motor starts to rotate immidiately. 2. READY indicator lights in about 0.5 seconds.
5. Stepping (Confirm the step rate with oscilloscope or counter)	1. Heads don't move toward outer track when heads are located on track 00. 2. When the heads is set to any track other than Track 00, Track 00 indicator does not light.
6. Track Positioning (Measure TS-1,2)	1. Such a Cat's Eye pattern signal as shown in figure D-1 can be obtained when heads access Track 40. (The oscilloscope is triggered by INDEX signal.) 2. HEAD SELECT switch is turned to side 1. Such a Cat's Eye pattern signal as shown in figure D-1 can be obtained when heads access Track 40. 3. Measure the amplitude (A) and (B) in figure D-1. Calculate the off track value, referring to the Specifications of the Standard Disk which is attached as a appendix of this manual.  **Figure D-1. Cat's Eye Pattern**
7. Motor Speed	1. The motor speed can be measured with universal counter using INDEX pulses. It should be within 200msec±3msec.

8. Index Position (Measure TS-1,2)	1. The following waveform can be obtained on Track 02.  **Figure D-2. Index Phase**
9. Track 00 signal	1. Move the heads to Track 01. 2. Move the heads by one step towards outer track. The following timing can be obtained. 
10. Azimuth (Measure TS-1,2)	1. Azimuth of heads can be obtained on Track 02, (TS1,2) Refer to the specifications of the Standard Disk. Azimuth should be within ±30'.
11. Time Margin (Window Margin)	1. Time Margin can be obtained with FTS-1. Time Margin on Track 79 (side 1/0) should be more than 0.6μsec.

2-3-2 Check Point to Abnormal Operation

Step	Abnormal Operation for each step	Check Point (defective place)	Remarks
Power on	1. The heads don't move to Track 00.	1. Track 00 sensing circuit. 2. Cassette in signal.	TS-8 TS-9
	2. The heads are stepped out but they are idling around the outer most track.	1. Track 00 sensing circuit.	TS-8
	3. The heads movement is not constant.	1. Drive system of stepping motor.	Source voltage is lower than 4.4 volts.
	4. The spindle motor does not stop to rotating.	1. Drive system of spindle motor.	
"MOTOR ON" switch on	1. The spindle motor does not rotate.	1. Drive system of spindle motor.	
Eject the disk	1. The spindle motor does not stop to rotating. 2. Disk is not ejected smoothly.	1. Diskette in signal. 2. Mechanism is no good.	TS-9
Load the disk	1. The spindle motor does not start to rotating.	1. Diskettte in signal 2. INDEX signal.	TS-9
Stepping	1. The step operation does not function at all, or it is not smoothly functioning.	1. Drive system of stepping motor or stepping motor itself. 2. The harness (i.e. The Track 00 sensor) is internally attached to other mounting parts. 3. Obstacles are attached to the slide guide shaft.	
Track positioning	1. The ration of the left to right signals does not meet the specification.	1. A voltage of VCC is lower than 4.4 volts. 2. Radial alignment is incomplete.	TS-1, 2
	2. No signal appears	1. Read amplifier circuit. 2. Seek error.	TS-1,2 Refer to 2-2-3
Motor speed	1. The motor speed does not meet the specification	1. The disk motor 2. The heads compliance.	
INDEX position	1. When the diskette is loaded twice or more, position is varied $\pm$ 100μsec or more.	1. The chucking mechanism of the disk motor is defective.	
	2. When the diskette is loaded twice or more, position is varied less than $\pm$ 100μsec. The shifted position, however, does not meet the specification.	1. The INDEX phase is mis-adjusted.	
TRACK 00 signal	1. Track 00 signal does not meet the specification.	1. The Track 00 sensor positioning is improper.	
Azimuth	1. Azimuth does not meet the specification.	1. The heads does not assembled correctly.	
Time Margin	1. Time Margin does not meet the specification.	1. PCB is wrong. 2. Carriage is no good.	

2-4 FINAL CHECK

Final check should be done using test system.
Check list is shown below.

1) Format with the other FDD.
2) Do the Read/Write test with random seek.
3) Ten surfaces should be tested. (One surface = All tracks, both sides)
4) No error should be caused on the test.

3. Parts Replacement

3-1 P.C.B. REPLACEMENT

3-1-1 Removal

a) If shield cover is installed, remove the one screw which fastens shield cover to the frame.
b) Remove the two screws which fasten PCB to the frame.
c) Remove the connectors except Head Cable Connector
   It is easy for removal to use small screw driver for removal.
d) Move the PCB with care not to apply excessive force to the Head cable, and then remove the Head cable connectors.

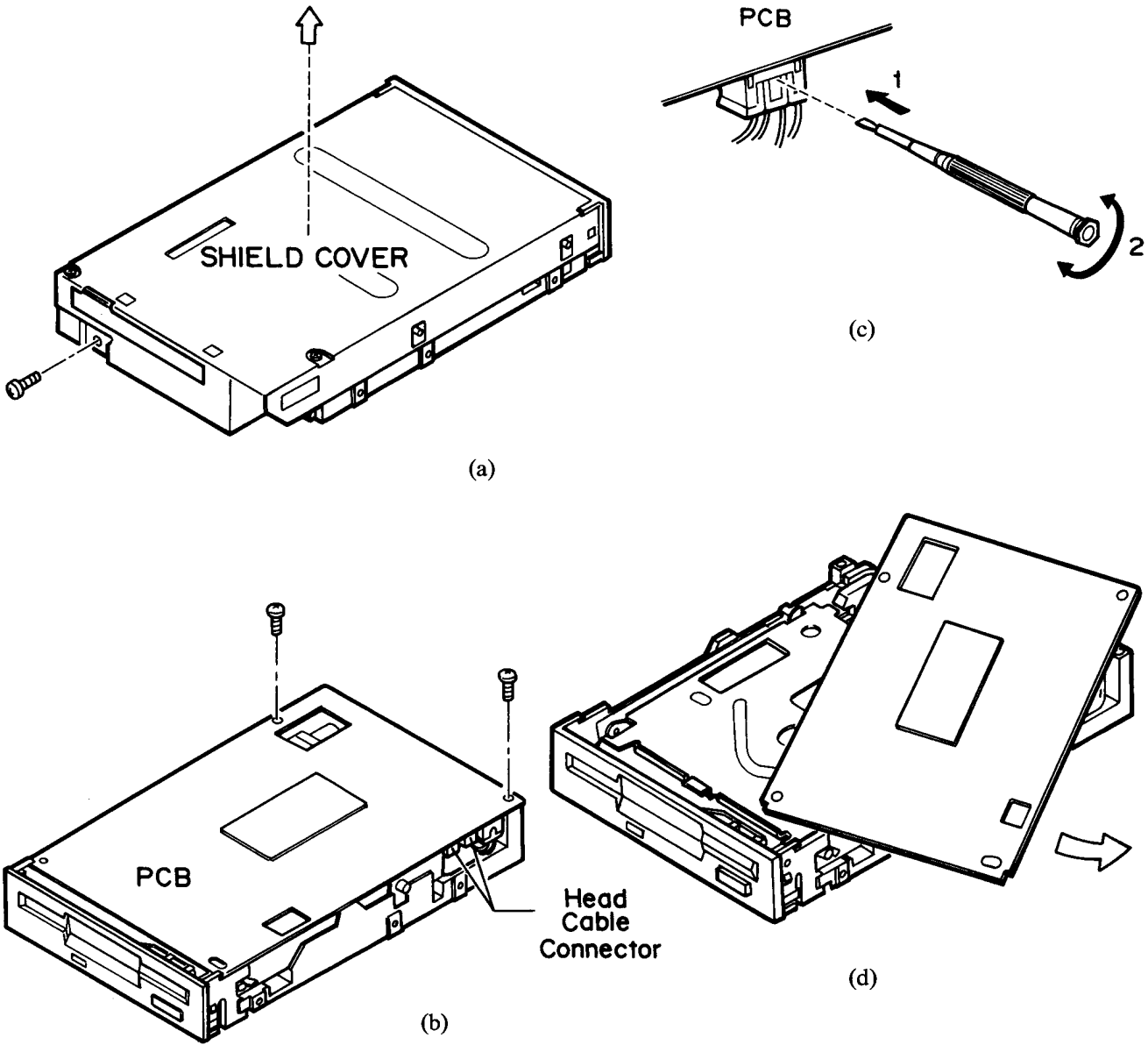


Figure D-3. P.C.B Replacement

3-1-2 Installation

a) Set the respective connectors to the PCB.
b) Place the PCB on the frame of FDD.
c) Fasten the PCB with two screws.

3-2. FRONT PANEL REPLACEMENT

3-2-1 Removal

a) Remove the PCB (Refer to 3-1-1)
b) Remove the Eject Button.
c) Remove the Front Panel.

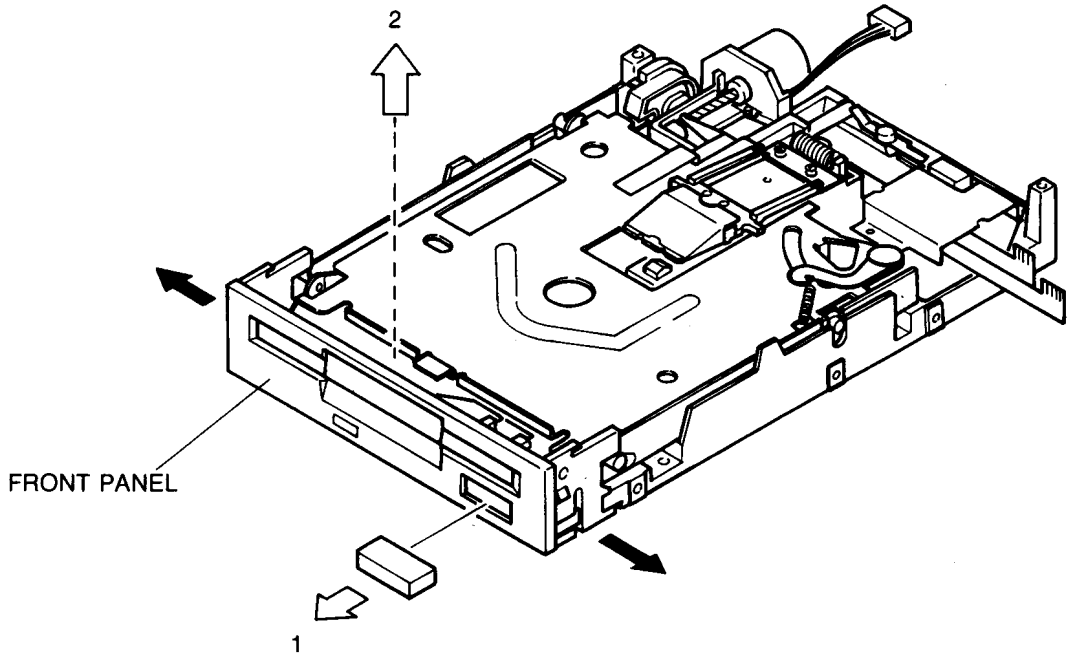


Figure D-4. Front Panel Replacement

3-2-2 Installation

a) Install the Front Panel.
b) Install the Eject Button.
c) Install the PCB (Refer to 3-1-2).

3-3 CARRIER REPLACEMENT

3-3-1 Removal

a) Remove the PCB. (Refer to 3-1-1).
b) Remove the Front Panel. (Refer to 3-2-1)
c) Put a Head Protect Sheet between the heads.
d) Remove the Carrier pushing the Slide Plate. Do not apply any excessive force to Carriage and heads.

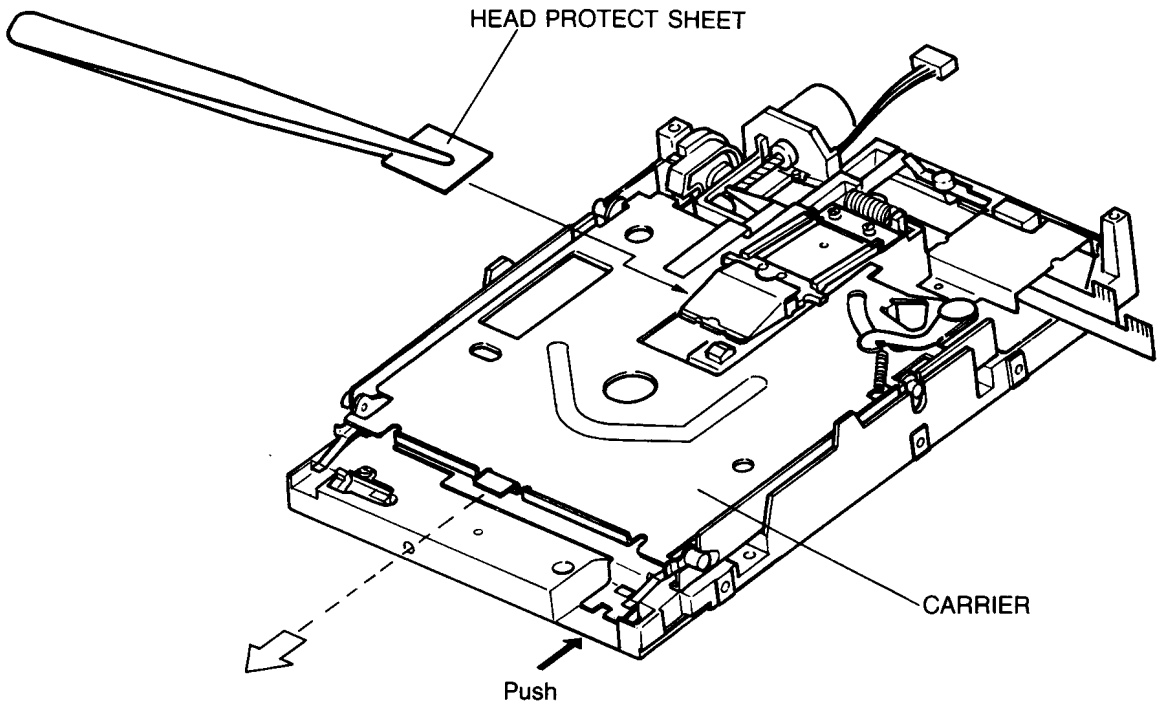


Figure D-5. Carrier Replacement

3-3-2 Installation

a) Install the Carrier. (Set the Carrier to the damper.) (Set the Carrier under the upper head.)
b) Remove the Head Protect Sheet.
c) Install the Front Panel. (Refer to 3-1-2)
d) Install the PCB. (Refer to 3-2-2)

3-4 SLIDE PLATE REPLACEMENT

3-4-1 Removal

a) Remove the PCB. (Refer to 3-1-1).
b) Remove the Front Panel. (Refer to 3-2-1)
c) Remove the Carrier. (Refer to 3-3-1)
d) Remove two springs which connect Slide Plate and Frame.
e) Remove the Slide Plate.

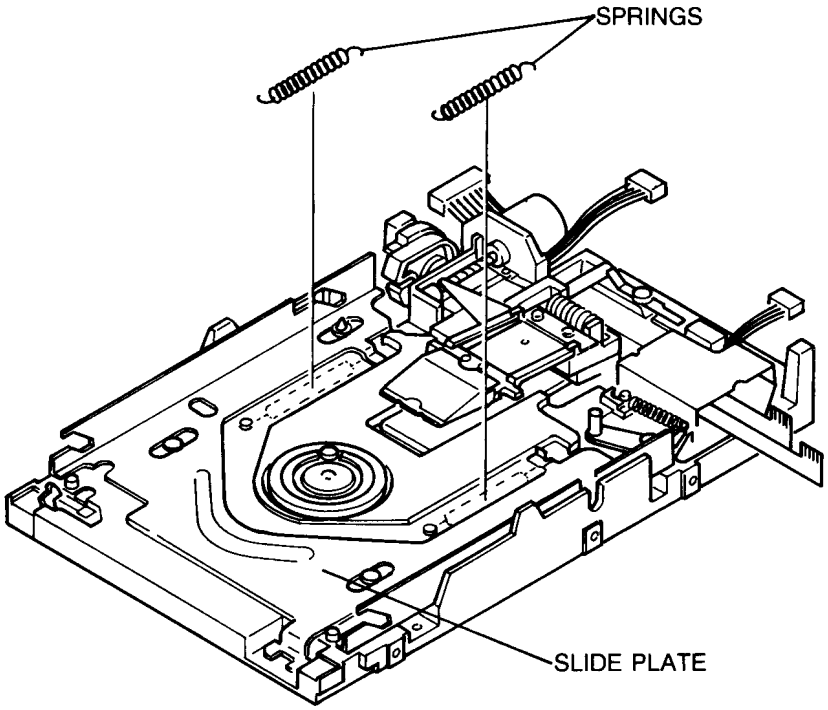


Figure D-6. Slide Plate Replacement

3-4-2 Installation

a) Install the Slide Plate.
b) Install the two springs.
c) Install the Carrier. (Refer to 3-3-2)
d) Install the Front Panel. (Refer to 3-2-2)
e) Install the PCB. (Refer to 3-1-2)

4. Adjustment

4-1 Head Alignment

a) Measure the Cat's Eye Pattern. (Refer to 2-3-1,-6)
b) Loosen the two screws for stepping motor.
c) Adjust the head alignment within $\pm 9\mu m$ by moving the stepping motor by hand.
(Cat's Eye ratio should be more than o.9)
d) Fasten the screws for stepping motor.
e) Confirm the head alignment again.

Figure D-7. Head Alignment

4-2 Index Alignment

a) Measure Index Alignment. (Refer to 2-3-1, -8)
b) Adjust the Index Alignment for within 500 $\pm$ 200 μsec by sliding the INDEX sensor. (Screw should be loosen slightly.)
c) Tighten the screw and confirm Index Alignment again.

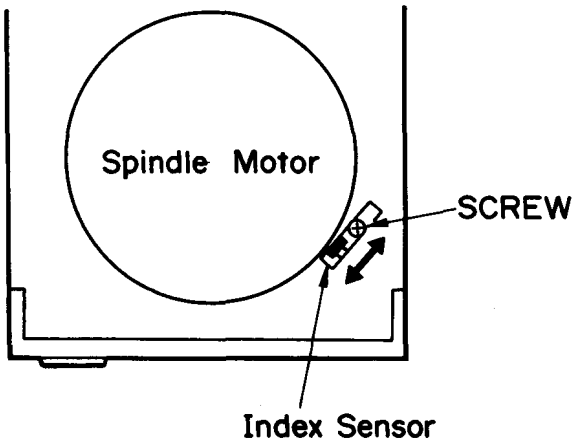


Figure D-8. Index Alignment

E. CHARACTER CODE TABLE

Decimal	Hex	Binary	Printed Character	Keystrokes
0	00	00000000	Space	CTRL 2
1	01	00000001	☺	CTRL A
2	02	00000010	☻	CTRL B
3	03	00000011	♥	CTRL C
4	04	00000100	♦	CTRL D
5	05	00000101	♣	CTRL E
6	06	00000110	♠	CTRL F
7	07	00000111	•	CTRL G
8	08	00001000	◘	CTRL H
9	09	00001001	○	CTRL I
10	0A	00001010	◙	CTRL J
11	0B	00001011	♂	CTRL K
12	0C	00001100	♀	CTRL L
13	0D	00001101	♪	CTRL M
14	0E	00001110	♫	CTRL N
15	0F	00001111	☼	CTRL O
16	10	00010000	►	CTRL P
17	11	00010001	◄	CTRL Q
18	12	00010010	↕	CTRL R
19	13	00010011	‼	CTRL S
20	14	00010100	¶	CTRL T
21	15	00010101	§	CTRL U
22	16	00010110	▬	CTRL V
23	17	00010111	↨	CTRL W
24	18	00011000	↑	CTRL X
25	19	00011001	↓	CTRL Y
26	1A	00011010	→	CTRL Z
27	1B	00011011	←	CTRL [
28	1C	00011100	∟	CTRL \
29	1D	00011101	↔	CTRL]

Decimal	Hex	Binary	Printed Character	Keystrokes
30	1E	00011110	▲	CTRL 6
31	1F	00011111	▼	CTRL -
32	20	00100000	SPACE	Space Bar
33	21	00100001	!	!
34	22	00100010	"	"
35	23	00100011	#	#
36	24	00100100	$	$
37	25	00100101	%	%
38	26	00100110	&	&
39	27	00100111	'	'
40	28	00101000	(	(
41	29	00101001	)	)
42	2A	00101010	*	*
43	2B	00101011	+	+
44	2C	00101100	,	,
45	2D	00101101	-	-
46	2E	00101110	.	.
47	2F	00101111	/	/
48	30	00110000	0	0
49	31	00110001	1	1
50	32	00110010	2	2
51	33	00110011	3	3
52	34	00110100	4	4
53	35	00110101	5	5
54	36	00110110	6	6
55	37	00110111	7	7
56	38	00111000	8	8
57	39	00111001	9	9
58	3A	00111010	:	:
59	3B	00111011	;	;
60	3C	00111100	<	<
61	3D	00111101	=	=

Decimal	Hex	Binary	Printed Character	Keystrokes
62	3E	00111110	>	>
63	3F	00111111	?	?
64	40	01000000	@	@
65	41	01000001	A	A
66	42	01000010	B	B
67	43	01000011	C	C
68	44	01000100	D	D
69	45	01000101	E	E
70	46	01000110	F	F
71	47	01000111	G	G
72	48	01001000	H	H
73	49	01001001	I	I
74	4A	01001010	J	J
75	4B	01001011	K	K
76	4C	01001100	L	L
77	4D	01001101	M	M
78	4E	01001110	N	N
79	4F	01001111	O	O
80	50	01010000	P	P
81	51	01010001	Q	Q
82	52	01010010	R	R
83	53	01010011	S	S
84	54	01010100	T	T
85	55	01010101	U	U
86	56	01010110	V	V
87	57	01010111	W	W
88	58	01011000	X	X
89	59	01011001	Y	Y
90	5A	01011010	Z	Z
91	5B	01011011	[	[
92	5C	01011100	\	\
93	5D	01011101	]	]

Decimal	Hex	Binary	Printed Character	Keystrokes
94	5E	01011110	^	^
95	5F	01011111	-	-
96	60	01100000	`	`
97	61	01100001	a	a
98	62	01100010	b	b
99	63	01100011	c	c
100	64	01100100	d	d
101	65	01100101	e	e
102	66	01100110	f	f
103	67	01100111	g	g
104	68	01101000	h	h
105	69	01101001	i	i
106	6A	01101010	j	j
107	6B	01101011	k	k
108	6C	01101100	l	l
109	6D	01101101	m	m
110	6E	01101110	n	n
111	6F	01101111	o	o
112	70	01110000	p	p
113	71	01110001	q	q
114	72	01110010	r	r
115	73	01110011	s	s
116	74	01110100	t	t
117	75	01110101	u	u
118	76	01110110	v	v
119	77	01110111	w	w
120	78	01111000	x	x
121	79	01111001	y	y
122	7A	01111010	z	z
123	7B	01111011	{	{
124	7C	01111100	¦	¦
125	7D	01111101	}	}

Decimal	Hex	Binary	Printed Character	Keystrokes
126	7E	01111110	~	~
127	7F	01111111	△	CTRL ←
128	80	10000000	Ç	ALT 128
129	81	10000001	ü	ALT 129
130	82	10000010	é	ALT 130
131	83	10000011	â	ALT 131
132	84	10000100	ä	ALT 132
133	85	10000101	à	ALT 133
134	86	10000110	å	ALT 134
135	87	10000111	ç	ALT 135
136	88	10001000	ê	ALT 136
137	89	10001001	ë	ALT 137
138	8A	10001010	è	ALT 138
139	8B	10001011	ï	ALT 139
140	8C	10001100	î	ALT 140
141	8D	10001101	ì	ALT 141
142	8E	10001110	Ä	ALT 142
143	8F	10001111	Å	ALT 143
144	90	10010000	È	ALT 144
145	91	10010001	æ	ALT 145
146	92	10010010	Æ	ALT 146
147	93	10010011	ô	ALT 147
148	94	10010100	ö	ALT 148
149	95	10010101	ò	ALT 149
150	96	10010110	û	ALT 150
151	97	10010111	ù	ALT 151
152	98	10011000	ÿ	ALT 152
153	99	10011001	Ö	ALT 153
154	9A	10011010	Ü	ALT 154
155	9B	10011011	¢	ALT 155
156	9C	10011100	£	ALT 156
157	9D	10011101	¥	ALT 157

Decimal	Hex	Binary	Printed Character	Keystrokes
158	9E	10011110	Pt	ALT 158
159	9F	10011111	ƒ	ALT 159
160	A0	10100000	á	ALT 160
161	A1	10100001	í	ALT 161
162	A2	10100010	ó	ALT 162
163	A3	10100011	ú	ALT 163
164	A4	10100100	ñ	ALT 164
165	A5	10100101	Ñ	ALT 165
166	A6	10100110	ª	ALT 166
167	A7	10100111	º	ALT 167
168	A8	10101000	¿	ALT 168
169	A9	10101001	⌐	ALT 169
170	AA	10101010	¬	ALT 170
171	AB	10101011	½	ALT 171
172	AC	10101100	¼	ALT 172
173	AD	10101101	¡	ALT 173
174	AE	10101110	«	ALT 174
175	AF	10101111	»	ALT 175
176	B0	10110000	▒	ALT 176
177	B1	10110001	▒	ALT 177
178	B2	10110010	▓	ALT 178
179	B3	10110011	│	ALT 179
180	B4	10110100	┤	ALT 180
181	B5	10110101	╡	ALT 181
182	B6	10110110	╢	ALT 182
183	B7	10110111	╖	ALT 183
184	B8	10111000	╕	ALT 184
185	B9	10111001	╣	ALT 185
186	BA	10111010	║	ALT 186
187	BB	10111011	╗	ALT 187
188	BC	10111100	╝	ALT 188

Decimal	Hex	Binary	Printed Character	Keystrokes
189	BD	10111101	╜	ALT 189
190	BE	10111110	╛	ALT 190
191	BF	10111111	┐	ALT 191
192	C0	11000000	└	ALT 192
193	C1	11000001	┴	ALT 193
194	C2	11000010	┬	ALT 194
195	C3	11000011	├	ALT 195
196	C4	11000100	─	ALT 196
197	C5	11000101	┼	ALT 197
198	C6	11000110	╞	ALT 198
199	C7	11000111	╟	ALT 199
200	C8	11001000	╚	ALT 200
201	C9	11001001	╔	ALT 201
202	CA	11001010	╩	ALT 202
203	CB	11001011	╦	ALT 203
204	CC	11001100	╠	ALT 204
205	CD	11001101	═	ALT 205
206	CE	11001110	╬	ALT 206
207	CF	11001111	╧	ALT 207
208	D0	11010000	╨	ALT 208
209	D1	11010001	╤	ALT 209
210	D2	11010010	╥	ALT 210
211	D3	11010011	╙	ALT 211
212	D4	11010100	╘	ALT 212
213	D5	11010101	╒	ALT 213
214	D6	11010110	╓	ALT 214
215	D7	11010111	╫	ALT 215
216	D8	11011000	╪	ALT 216
217	D9	11011001	┘	ALT 217
218	DA	11011010	┌	ALT 218
219	DB	11011011	■	ALT 219

Decimal	Hex	Binary	Printed Character	Keystrokes
220	DC	11011100	▄	ALT 220
221	DD	11011101	▌	ALT 221
222	DE	11011110	▐	ALT 222
223	DF	11011111	▀	ALT 223
224	E0	11100000	α	ALT 224
225	E1	11100001	β	ALT 225
226	E2	11100010	Γ	ALT 226
227	E3	11100011	π	ALT 227
228	E4	11100100	Σ	ALT 228
229	E5	11100101	o	ALT 229
230	E6	11100110	μ	ALT 230
231	E7	11100111	γ	ALT 231
232	E8	11101000	Φ	ALT 232
233	E9	11101001	θ	ALT 233
234	EA	11101010	Ω	ALT 234
235	EB	11101011	σ	ALT 235
236	EC	11101100	∞	ALT 236
237	ED	11101101	ϕ	ALT 237
238	EE	11101110	ϵ	ALT 238
239	EF	11101111	$\cap$	ALT 239
240	F0	11110000	$\equiv$	ALT 240
241	F1	11110001	$\pm$	ALT 241
242	F2	11110010	$\geq$	ALT 242
243	F3	11110011	$\leq$	ALT 243
244	F4	11110100	$\lceil$	ALT 244
245	F5	11110101	$\rfloor$	ALT 245
246	F6	11110110	$\div$	ALT 246
247	F7	11110111	$\approx$	ALT 247
248	F8	11111000	○	ALT 248
249	F9	11111001	●	ALT 249
250	FA	11111010	·	ALT 250

Decimal	Hex	Binary	Printed Character	Keystrokes
251	FB	11111011	√	ALT 251
252	FC	11111100	n	ALT 252
253	FD	11111101	2	ALT 253
254	FE	11111110	■	ALT 254
255	FF	11111111	BLANK	ALT 255

F. DESCRIPTION OF I/O COMMANDS

Device Address Map

DMA CONTROLLER

Address	Bit	Bit data	Description
08H (Command-Register)	0	0/1	Memory to memory transfer disable/enable
	1	0/1 X	Channel 0 address hold disable/enable In case of bit 0=0
	2	0/1	Controller enable/disable
	3	0/1 X	Normal/Compressed timing In case of bit 0=1
	4	0/1	Fixed/Rotating Priority
	5	0 1 X	Normal write pulse Extended write selection In case of bit 3=1
	6	0/1	DREQ sense active high/low
	7	0/1	DACK sense active high/low
09H (Request-Register)	0,1	00 01 10 11	Selection of channel 0 Selection of channel 1 Selection of channel 2 Selection of channel 3
	2	0/1	Preset/Set of request bit
	3 ~ 7	X	X
0AH (Mask-Register)	0,1	00 01 10 11	Selection of mask bit of channel 0 Selection of mask bit of channel 1 Selection of mask bit of channel 2 Selection of mask bit of channel 3
	2	0/1	Clear/Set of mask bit
	3 ~ 7	X	X
	All four bits of the mask register can be written also by a single command		
	0	0/1	Clear/Set mask bit of channel 0
	1	0/1	Clear/Set mask bit of channel 1
	2	0/1	Clear/Set mask bit of channel 2
	3	0/1	Clear/Set mask bit of channel 3
	4 ~ 7	X	X

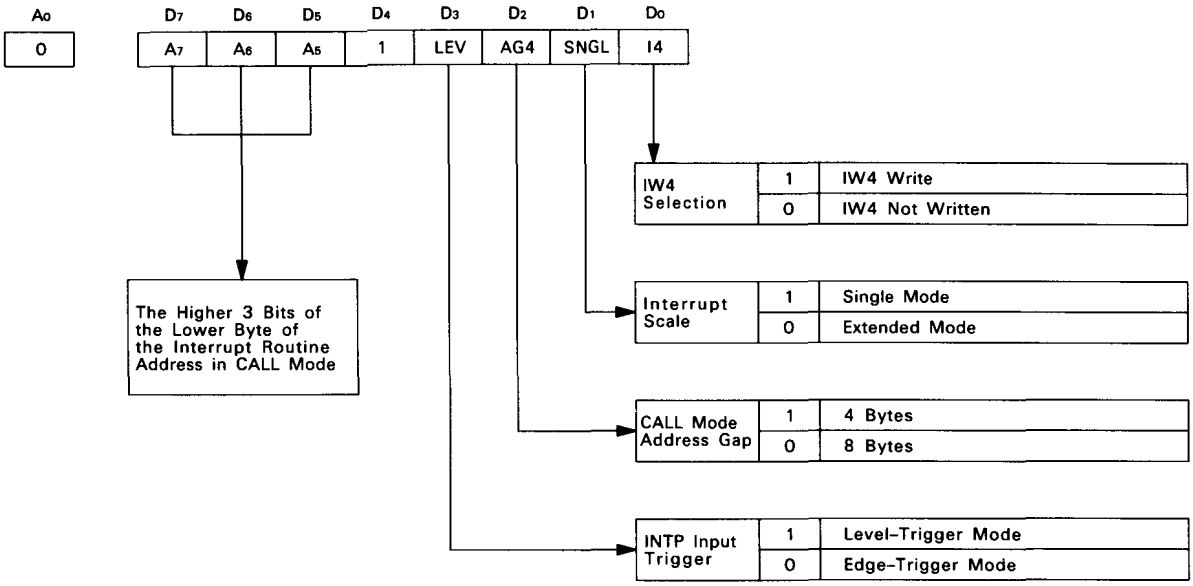
Address	Bit	Bit data	Description
0BH (Mode-Register)	0,1	00 01 10 11	Selection of channel 0 Selection of channel 1 Selection of channel 2 Selection of channel 3
	2,3	00 01 10 11 XX	Verify transfer Write transfer (I/O to Memory) Read transfer (Memory to I/O) Illegal In case of bit 6,7=11
	4	0/1	Auto initialize disable/enable
	5	0/1	Address increment/decrement
	6,7	00 01 10 11	Demand mode Single mode Block mode Cascade mode
0CH (software command)	0 ~ 7	X	Clear First/Last flip flop
0DH (software command)	0 ~ 7	X	Read of temporary register/Master clear
0EH (software command)	0 ~ 7	X	Clear Mask register
0FH (software command)	0 ~ 7	X	All Mask register

INTERRUPT CONTROLLER

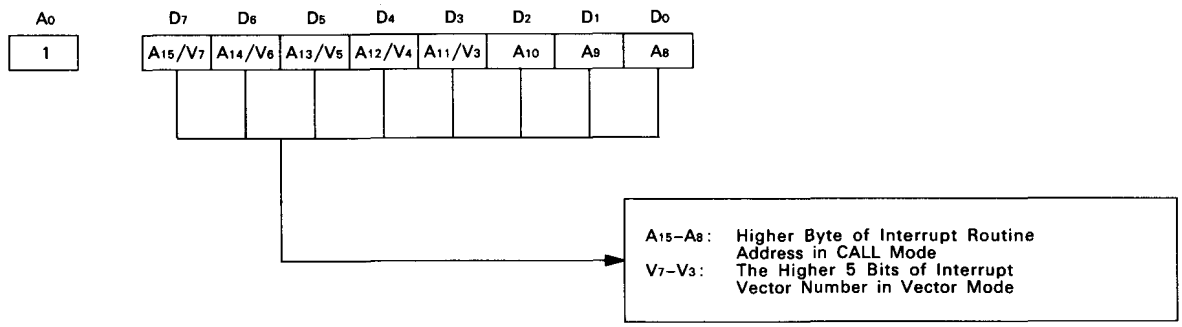
Address	Bit	Bit data	Description
020H	0 ~ 7		IRR & ISR
021H	0 ~ 7		IMR

Initialization Word Format

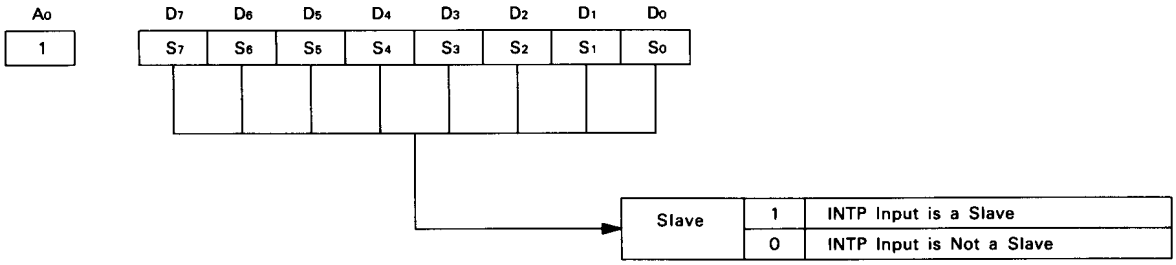
IW1 (Initialization Word 1)



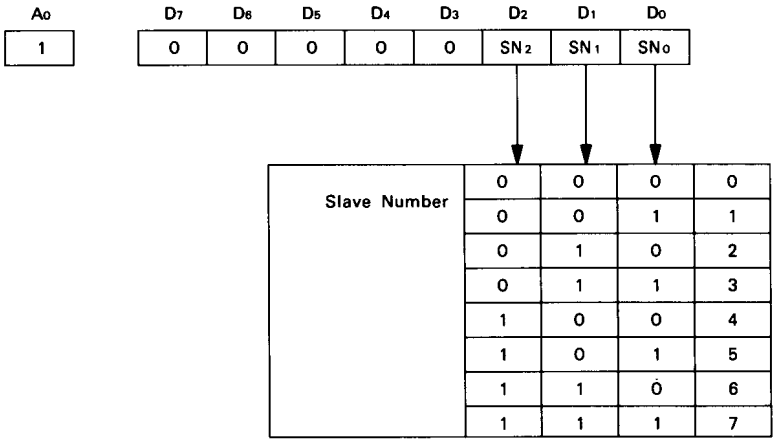
IW2 (Initialization Word 2)



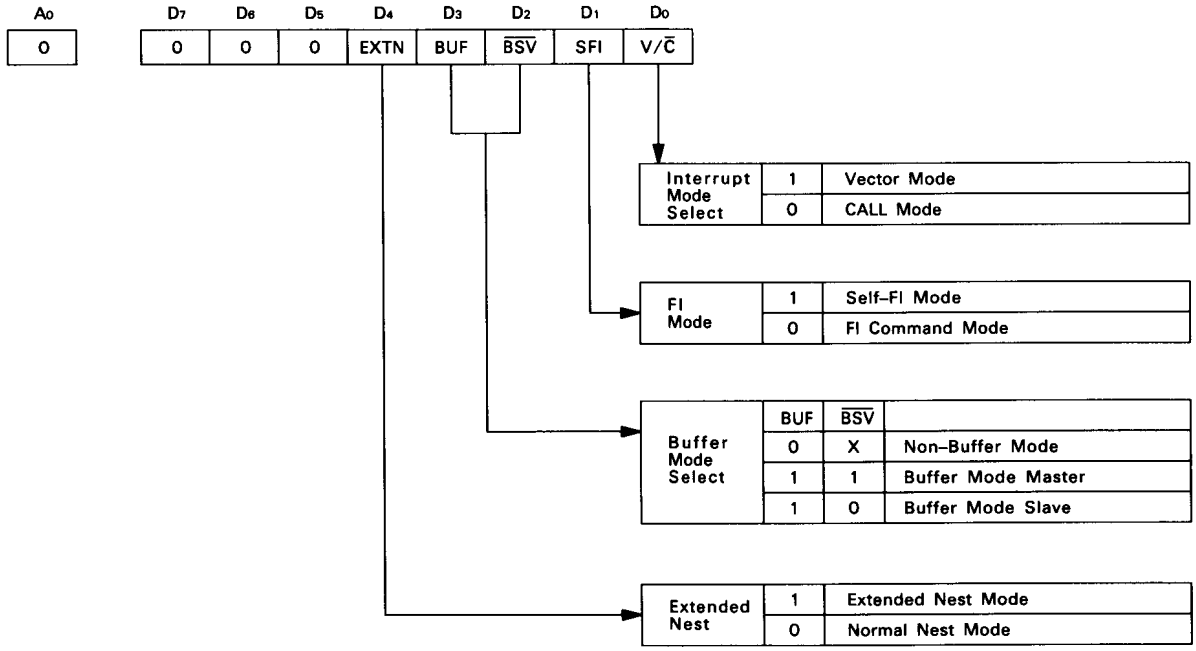
IW3 (Initialization Word 3) Masler Mode



IW3 (Initialization Word 3) Slave Mode

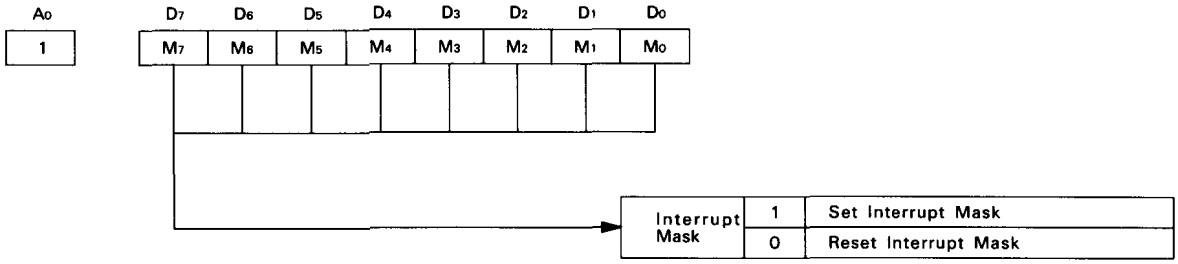


IW4 (Initialization Word 4)

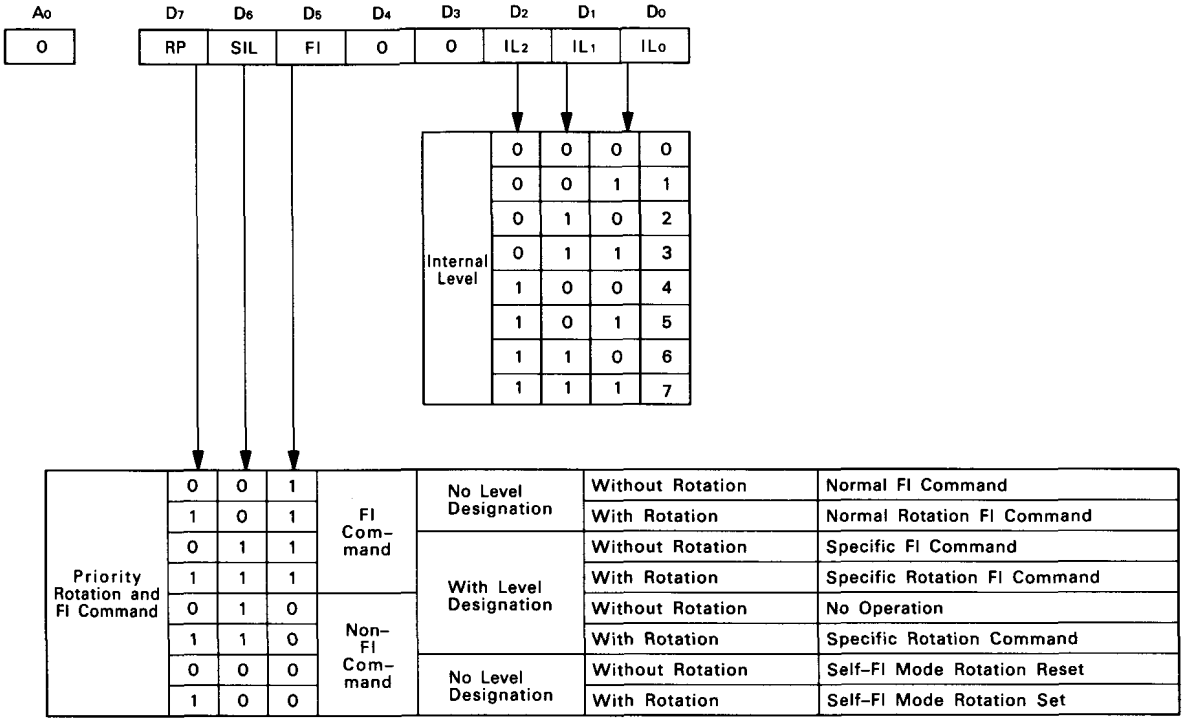


Command Word Format

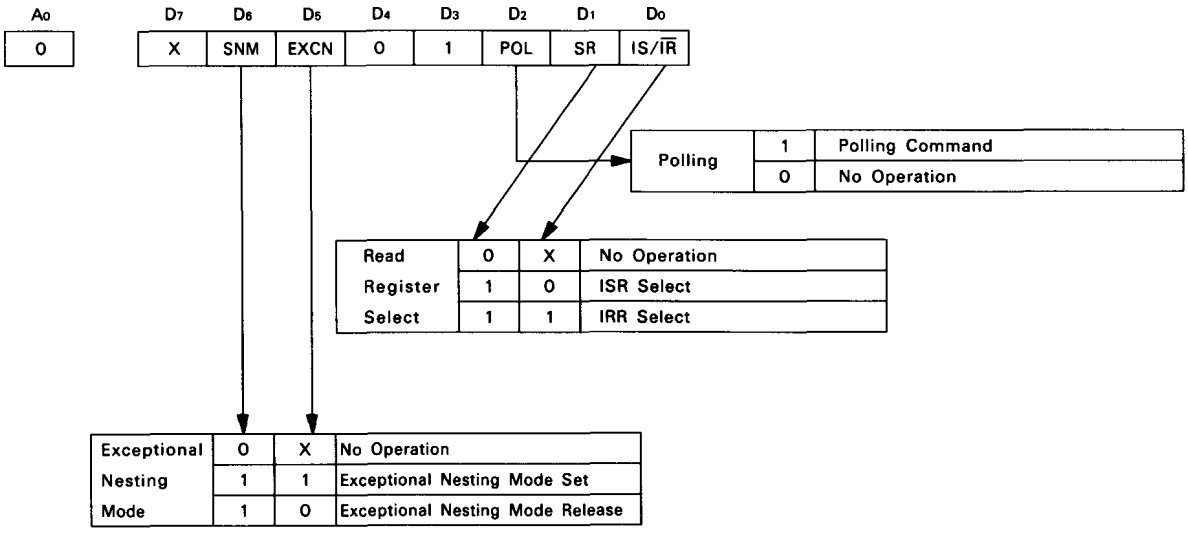
IMW (Interrupt Mask Word)



PFCW (Priority Finish and Control Word)



MCW (Mode Control Word)



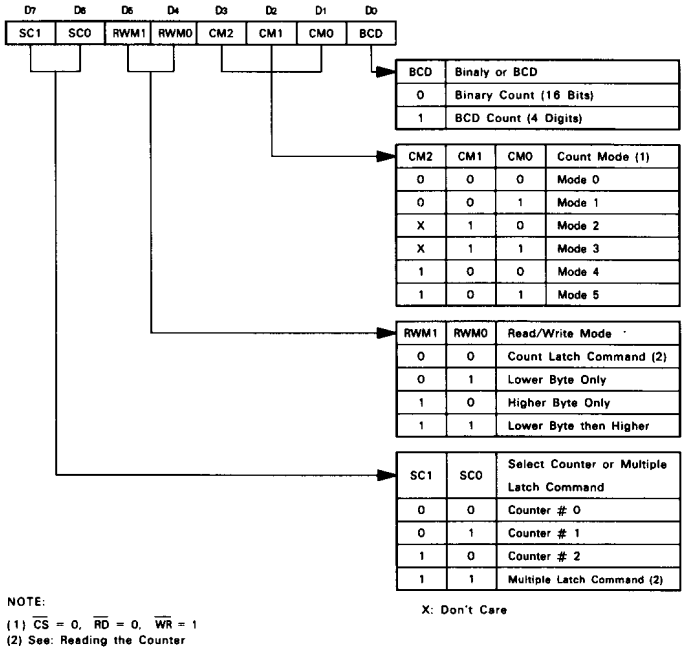
TIMER/COUNTER

The program must write a control command to set the counter mode and write the count data that determines the length of the count operation.

Write Operations ($\overline{CS}$=0, $\overline{RD}$=1, $\overline{WR}$=0)

Address	A1	A0	Write Target
40H	0	0	Counter 0
41H	0	1	Counter 1
42H	1	0	Counter 2
43H	1	1	Control word register

Control Register Format



Read/Write Mode and Count Write

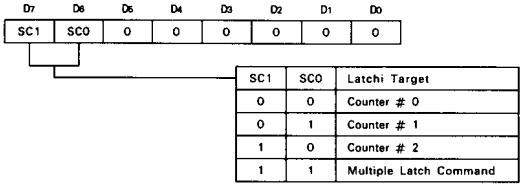
Read/Write Mode	No. of Writes	Count Register	
		Higher Byte	Lower Byte
Low 1-byte	1	00H	nnH
High 1-byte	1	nnH	00H
Low/High 2-byte	2	nnH (2nd write)	nnH (1st write)

nnH = Two-digit hexadicimal value

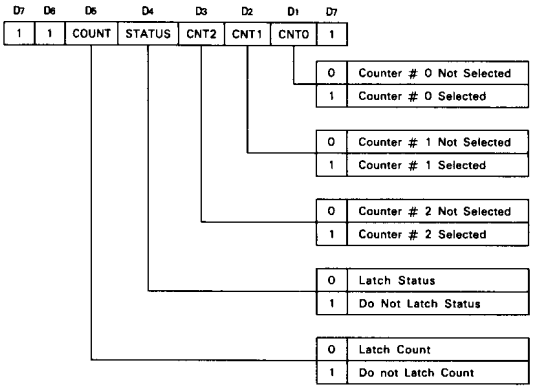
Read Operations ($\overline{CS}$=0, $\overline{RD}$=0, $\overline{WR}$=1)

Address	A1	A0	Read Target
40H	0	0	Counter 0
41H	0	1	Counter 1
42H	1	0	Counter 2

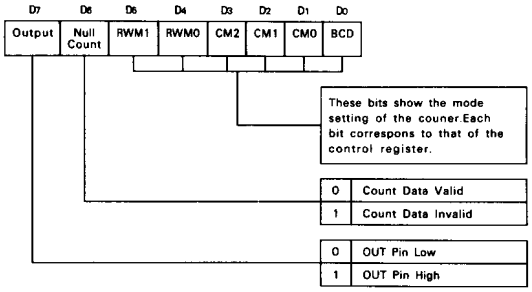
Control Register Format for Count Latch Command



Control Regester Format for Multiple Latch Command



Status Data



KEYBOARD/SENSE/CONTROL

Address	Bit	Bit data	Description
060H	0	0/1	Keyboard Bit 0
	1	0/1	Keyboard Bit 1
	2	0/1	Keyboard Bit 2
	3	0/1	Keyboard Bit 3
	4	0/1	Keyboard Bit 4
	5	0/1	Keyboard Bit 5
	6	0/1	Keyboard Bit 6
	7	0/1	Keyboard Bit 7
061H	0	1/0	Gate A Timer Chip for Speaker Tone Output
	1	1/0	Enable/disable speaker
	2	X	———
	3	1/0	Read High SW or Read Low SW
	4	X	———
	5	X	———
	6	1/0	Keyboard buffering SW
	7	1/0	Keyboard interrupt reset
062H	0	1/0	System status of hardware
	1	1/0	System status of hardware
	2	1/0	System status of hardware
	3	1/0	System status of hardware
	4	X	———
	5	1/0	To test Timer output
	6	0	I/O channel check (always low level)
	7	0	RAM Parity check (always low level)

REAL TIME CLOCK

Address allocation of MODE 00 (Note 1)

Address	MODE	MODE 00				
	A3 ~ A1	Contents	D3	D2	D1	D0
070H	0	1-sec counter				
071H	1	10-sec counter	X			
072H	2	1-min counter				
073H	3	10-min counter	X			
074H	4	1-hour counter				
075H	5	10-hour counter (Note 2)	X	X		
076H	6	Day-of-the-weed counter	X			
077H	7	1-day counter				
078H	8	10-day counter	X	X		
079H	9	1-month counter				
07AH	A	10-month counter	X	X	X	
07BH	B	1-year counter				
07CH	C	10-year counter				
07DH	D	MODE Register	Timer EN	Alarm EN	MODE selector	
					M1	M2
07EH	E	Test Register	Test 3	Test 2	Test 1	Test 0
07FH	F	RESET Controller	$\overline{\text{1Hz ON}}$	$\overline{\text{16Hz ON}}$	Timer RESET	Alarm RESET

X indicates that the counter may take any value during write operation, but always be 0 when read out.

(Note 1) MODE 00 is set by writing data (X, X, 0, 0) to address 07DH.

(Note 2) Bit 1 of the 10-hour counter should be as follows when the 12-hour system is selected:

D1 = 1 (PM)

D1 = 0 (AM)

Address allocation of MODE 01 (Note 1)

Address	MODE	MODE 01				
	A3 ~ A1	Contents	D3	D2	D1	D0
070H	0		X	X	X	X
071H	1		X	X	X	X
072H	2	Alarm 1-min register				
073H	3	Alarm 10-min register	X			
074H	4	Alarm 1-hour register				
075H	5	Alarm 10-hour register	X	X		
076H	6	Alarm day-of-the-week register	X			
077H	7	Alarm 1-day register				
078H	8	Alarm 10-day register	X	X		
079H	9		X	X	X	X
07AH	A	$\overline{\text{12-hour}}$/24-hour selector	X	X	X	
07BH	B	Leap-year counter	X	X		
07CH	C		X	X	X	X
07DH	D	MODE Register	Timer EN	Alarm EN	MODE selector	
					M1	M0
07EH	E	Test Register	Test 3	Test 2	Test 1	Test 0
07FH	F	RESET Controller	$\overline{\text{1Hz}}$ $\overline{\text{ON}}$	$\overline{\text{16Hz}}$ $\overline{\text{ON}}$	Timer RESET	Alarm RESET

(Note 1) MODE 01 is set by writing data (X, X, 0, 1) to address 07DH.

Address allocation of MODE 10 and 11 (Note 1)

Address	MODE A3 ~ A1	MODE 10 Contents				MODE 11 (RAM) Contents			
070H	0								
071H	1								
072H	2	block 10				block 11			
073H	3								
074H	4								
075H	5	4 bit				4 bit			
076H	6	X				X			
077H	7	13				13			
078H	8								
079H	9	RAM				RAM			
07AH	A								
07BH	B								
07CH	C								
07DH	D	Timer EN	Alarm EN	MODE selector		Timer EN	Alarm EN	MODE selector	
				M1	M0			M1	M0
07EH	E	Test 3	Test 2	Test 1	Test 0	Test 3	Test 2	Test 1	Test 0
07FH	F	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ ON	Timer RESET	Alarm RESET	$\overline{1Hz}$ $\overline{ON}$	$\overline{16Hz}$ $\overline{ON}$	Timer RESET	Alarm RESET

(Note 1) MODE 10 is set to by writing data (X, X, 1, 0) to address 07DH.
MODE 11 is set by writing data (X, X, 1, 1) to address 07DH. (MODE 10 and 11 are in RAM areas)

* Mode register (A3, A2, A1, A0) = (1, 1, 0, 1) = D

D3	D2	D1	D0	
Timer EN	Alarm EN	M1	M0	
		0	0	MODE 00: setting or reading time
		0	1	MODE 01: Setting or reading of Alarm data, 12/24 hour system, or leap year
		1	0	Writing to or reading Block 10 in RAM
		1	1	Writing to or reading Block 11 in RAM
				Set 1 to enable alarm output. Set 0 to disable alarm output (16Hz/1Hz clock signals not affected)
				Set 1 to start clock. Set 0 to stop seconds and subsequent counters.

* The leap-year counter registers a leap year when D1=D0=0. It simultaneously counts with the year counter.
* The $\overline{12\text{-hour}}$/24-hour selector sets the 12-hour system when D0=0 and the 24-hour system when D0=1. PM or AM is selected when D1 in the 10-hour counter is 1 or 0, respectively.
* Reset controller 16Hz/1Hz clock register.
  (A3, A2, A1, A0) = (1, 1, 1, 1) = F
  D0 = 1: resets all alarm registers and internal Alarm F/Fs.
  D1 = 1: resets the 15-stage dividers before the seconds register.
  D2 = 0: switches on the 16Hz clock pulse generated from the $\overline{ALARM}$ terminal.
  D3 = 0: switches on the 1Hz clock pulse generated from the $\overline{ALARM}$ terminal.
* Addresses 070H ~ 07DH: able to read and write.
* Addresses 07EH ~ 07FH: only able to write and 0H always appears when read out.

DMA PAGE REGISTER

Address	Bit	Bit data	Description
080H	———	———	Not used
081H			DMA Page Register for DMA channel 2
	0	1/0	Address A16
	1	1/0	Address A17
	2	1/0	Address A18
	3	1/0	Address A19
	4 ~ 7	X	X
082H			DMA Page Register for DMA channel 3
	0	1/0	Address A16
	1	1/0	Address A17
	2	1/0	Address A18
	3	1/0	Address A19
	4 ~ 7	X	X
083H			DMA Page Register for DMA channel 1
	0	1/0	Address A16
	1	1/0	Address A17
	2	1/0	Address A18
	3	1/0	Address A19
	4 ~ 7	X	

NMI MASK REGISTER

Address	Bit	Bit data	Description
0A0H	7	0	NMI Mask Register

SYSTEM STATUS REGISTER

Refer to 4-13

PRINTER CONTROL

Address	Bit	Bit data	Description
378H (Printer Data Output Port)	0	1	Data Bit 0
	1	1	Data Bit 1
	2	1	Data Bit 2
	3	1	Data Bit 3
	4	1	Data Bit 4
	5	1	Data Bit 5
	6	1	Data Bit 6
	7	1	Data Bit 7
379H (Printer Status Port)	0	———	———
	1	———	———
	2	———	———
	3	0	Error
	4	1	Select
	5	1	P. End (Out of Paper)
	6	0	Acknowledge
	7	1	Busy
37AH (Printer Control Port)	0	0	Strobe
	1	0	Auto Feed
	2	0	Initialize Printer
	3	0	Select Input
	4	1	IR0 Enable
	5	———	———
	6	———	———
	7	———	———

VIDEO CONTROLLER

The following I/O devices are defined within the LCDC.

ADDRESS					DATA								R/W	FUNCTION OF REGISTER
HEX	3	2	1	0	7	6	5	4	3	2	1	0		
3D (0,2,4,6)	0	X	X	0	X	X	X	A4	.	.	.	A0	W	6845 ADDRESS REG.
3D (1,3,5,7)	0	X	X	1	D7	.	.	.	.	.	.	D0	R/W	6845 DATA REG.
3D 8	1	0	0	0	D7	.	.	.	.	.	.	D0	R/W	MODE CONT/ID REG.
3D 9	1	0	0	1	X	X	D5	.	.	.	.	D0	W	COLOR SELECT REG.
3D A	1	0	1	0	X	X	X	D4	.	.	.	D0	R	STATUS REGISTER
3D B	1	0	1	1	X	X	X	X	X	X	X	X	W	CLEAR LIGHT PEN
3D C	1	0	1	0	X	X	X	X	X	X	X	X	W	PRESET LIGHT PEN
3D D	1	1	0	1	P	D6	.	.	.	.	.	D0	W	REGISTER BANK ADR.
3D E	1	1	1	0	D7	.	.	.	.	.	.	D0	W	REGISTER BANK DATA
3D F	1	1	1	1	X	X	X	X	X	D2	.	D0	W	DISPLAY PAGE

I/O REGISTER SUMMARY

The "X" means "don't care" bit. Address "3D8" and "3DA" are partially expanded registers. Address "3DD", "3DE", and "3DF" are new expanded registers.

3D8H (MODE CONT/ID REGISTER)

BIT	NAME	FUNCTION
0	80 × 25 A/N	80 × 25 ALPHA-NUMERIC
1	320 × 200 GR	COLOR GRAPHICS (320 × 200)
2	B&W	B&W SELECT
3	EN VIDEO	ENABLE VIDEO SIGNAL
4	HIGH RES.	HIGH RES. 640 × 200 GRAPHICS
5	BLINK	BLINK BIT ON ALPHA-NUMERIC MODE
6	160 × 200 GR	COLOR GRAPHICS (160 × 200 OR 640 × 200)
7	STAND-BY	STAND-BY MODE

MODE SELECT REGISTER

Bit 0 Selects between 40 × 25 and 80 × 25 alpha mode, a "1" sets it to 80 × 25 mode.

Bit 1 Selects between ALPHA mode and GRAPHICS mode, a "0" selects ALPHA modes. In graphics mode, the resolution is selected by combination of bit 4 and bit 6. Typically this bit "1" selects 320 × 200 Graphics mode.

Bit 2 Selects color or B&W mode, a "1" selects B & W mode, the composite-video's color-burst and chrominance (the CH signal) are disabled, leaving only the composite intensity levels for gray shades (the Y signal).

Bit 3 Enables the video signal at certain times when modes are being changed. The video signal should be disabled when changing modes. The video signal should be disabled when changing modes. A "1" enables the video signal.

Bit 4 Selects between high resolution 640 × 200 graphics modes and other resolution modes. When on, this bit selects 640 × 200 graphics modes and bit 6 selects between color and B & W mode.

Bit 5 When on, this bit will change the character background intensity to the blinking attribute function for ALPHA modes. When off, 16 background colors are available. For normal operation, this bit should be set to "1" to allow the blinking function.

3DAH (STATUS REGISTER)
The status register is a 5 bit read-only register. Its address is hex "3DA" of the four least significant bit of I/O address with "0" *IOSEL signal.

The following is a description of the register functions.

BIT	NAME	FUNCTION
0	DISP. EN.	DISPLAY ENABLE TIMING
1	LPD/MS1	LIGHT PEN TRIGGER SET or MOUSE SWITCH 1
2	LPS/MS0	LIGHT PEN SWITCH or MOUSE SWITCH 0
3	VSYNC	VERTICAL RETRACE TIMING
4	VIDEO	VIDEO DOT
5	———	NOT USED
6	———	NOT USED
7	———	NOT USED

STATUS REGISTER

Bit 0 When set, this bit indicates the display disabled timing signal on retracing.

Bit 1 When the Light Pen is selected, this bit "1" indicates that a positive-going edge from the light pen input has set the Light Pen Trigger flip-flop. This bit can be cleared by executing I/O OUT command to address hex "B" with any data.
When the Mouse is selected, this bit indicates the status of the Mouse Switch 1. The switch is not debounced and is not latched. When this bit is "0", the Mouse Switch 1 is "on".

Bit 2 This bit indicates the status of the Light Pen Switch or Mouse Switch 0. These switches are not debounced and are not latched. When this bit is "0", the switch which is selected by the expanded mode register, is "on".

Bit 3 When "1", this bit indicates the vertical retrace signal is "active", and if the Monochrome Adapter Mode is selected, this bit becomes the video-dot information as the same as bit 4.

3DDH, 3DEH (REGISTER BANK Address/Data)
All of the new expanded functions are implemented in the Register Bank.

This Register Bank includes the Sprite Pattern and its location data, Color Palette Register #0 to #15 data, display monitor configuration control data and memory configuration control data.

Registers within this bank are programmed by first writing a register address pointer to port hex "3DD" and then writing the data to port hex "3DE". The register address is incremented by one after a port hex "3DE" write operation.

The bit 7 of port hex "3DD" has a special function and is named the Protect Bit. When this bit sets, the bit 6 and bit 7 on the Mode Select Register can be active.

The following registers are defined on the Register Bank in the LCDC.

ADDRESS 346543210	DATA 7	6	5	4	3	2	1	0	REGISTER FUNCTION
0000000	D7	D6	D5	D4	D3	D2	D1	D0	Sprite Pattern data
———	I	I	I	I	I	I	I	I	
———	I	I	I	I	I	I	I	I	
0111111	D7	D6	D5	D4	D3	D2	D1	D0	
1000000	X	X	X	X	X	R2	R1	R0	Color Palette #0
1000001	X	G2	G1	G0	X	B2	B1	B0	
———	I	I	I	I	I	I	I	I	I
———	I	I	I	I	I	I	I	I	I
1011110	X	X	X	X	X	R2	R1	R0	Color Palette #15
1011111	X	G2	G1	G0	X	B2	B1	B0	
1100000	X	X	X	X	X	X	X	H8	Sprite Horizontal Location
1100001	H7	H6	H5	H4	H3	H2	H1	H0	
1100010	X	X	X	X	X	X	X	X	Sprite Vertical Location
1100011	V7	V6	V5	V4	V3	V2	V1	V0	
1100100	TEST1	TEST0	SS 2	SS 1	SS 0	S2 ON	S1 ON	BL	Test/Sprite Control
1100101	Mouse	SRAM	LCD	MONO	PAL	512/256	SCR1	SCR0	Monitor Control
1100110	–	MON	–	-	LCD	MODE	–	–	RAJ – MONO/LCD Control
	1	0	3	2	1	0	1	0	
1100111	16	PAGE	M-SEL	–		EH		–	Configuration Mode
	bit			4	3	2	1	0	
1101000	–	S2		–	–	S1		–	Sprite Color Select
	I	R	G	B	I	R	G	B	
1101001	–			CON				–	Control Data
	7	6	5	4	3	2	1	0	

REGISTER BANK SUMMARY

All registers are write-only register.

1. SPRITE

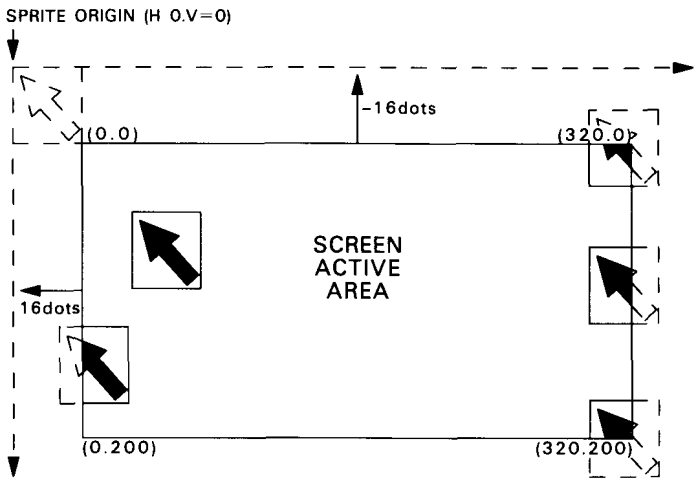
The SPRITE is used for the Cursor, it can be displayed as a AND & EXOR pattern and is a sliding pattern on the screen.

The Register Bank contains all the SPRITE informations.

The SPRITE 16 × 16 dot pattern is decided by SPRITE PATTERN DATA registers (hex 00-3F) and the displayed location is decided by the SPRITE HORIZONTAL LOCATION (hex 60, 61), and SPRITE VERTICAL LOCATION register (hex 62, 63). The blink mode and display enable/disable control data for the SPRITE are in the TEST/SPRITE CONTROL register (hex 64) and the color information are in the SPRITE COLOR SELECT register (hex 68).

The displayed location can be selected by dot units. The relation between origin point of SPRITE and display screen coordinates is shifted 16 dots to the left and upward of the 320 × 200 screen mode.

The actual displayed SPRITE pattern is an overlapped part with the screen display active area as in the following illustration.



2. Sprite Pattern Data

Two 16 × 16 dot patterns for the SPRITE can be defined in the Register Bank. One is the ANDing pattern, anded with the displayed screen pattern. The foreground color of this pattern is selected by the S1 SPRITE color of the SPRITE COLOR SELECT register (hex 68) in this Register Bank, and the background color of this pattern become white (all 1).

The second pattern is the EXORing pattern, which is exclusive-ored with the anded result of ANDing pattern and the screen pattern. The foreground color of this pattern is selected by the S2 SPRITE COLOR of SPRITE COLOR SELECT register and the background color of this pattern becomes transparent.

The following indicates the relation of the pattern and register data address.

Pattern Origin

D7	D0	D7	D0
00		01	
02		03	
.		.	
.		.	
1E		1F	

(HEX)

AND Pattern

Pattern Origin

D7	D0	D7	D0
20		21	
22		23	
.		.	
.		.	
3E		3F	

(HEX)

EXOR Pattern

3. Test/Sprite Control Register

This is an 8 bit write only-register. Its address is hex "64" within the Register Bank.

The following is a description of the Test/SPRITE CONTROL REGISTER function.

BIT	NAME	FUNCTION
0	BL	SPRITE BLINK ENABLED
1	S1 ON	SPRITE 1 (AND PATTERN) ENABLED
2	S2 ON	SPRITE 2 (EXOR PATTERN) ENABLED
3	SS 0	SMOOTH SCROLL OFFSET 0
4	SS 1	SMOOTH SCROLL OFFSET 1
5	SS 2	SMOOTH SCROLL OFFSET 2
6	TEST 0	SELECT TEST MODE
7	TEST 1	(MUST BE ZERO)

Bit 0 This bit, when set, enables the Sprite Blinking. Blinking period is 16 frame interval. This bit, when reset, will disable the blinking.

Bit 1 This bit, when set, enables the Sprite 1 function.

Bit 2 This bit, when set, enables the Sprite 2 function.

Bit 3-5 These three bits define the offset value. The screen raster will be shifted this number upward in the text mode.

Bit 6,7 These bits select the Test Mode of this controller. These bits can't be used and should be kept zero. These bits, if set, enable the operation and can't be used normally. These bits are cleared by the Vertical Sync signal.

This register is cleared by the RESET signal.

4. Monitor Control

This is an 8 bit write-only register. Its address is hex "65" within the Register Bank.

The following is a description of the Monitor Control Registers functions.

BIT	NAME	FUNCTION
0	SCR0	SELECT SCREEN VERTICAL LINE NUMBER 0
1	SCR1	SELECT SCREEN VERTICAL LINE NUMBER 1
2	512/256	SELECT SCREEN HORIZONTAL DOT NUMBER
3	PAL	SELECT PAL. SECAM/NTSC
4	MONO	SELECT MONOCHROME MONITOR/COLOR
5	LCD	SELECT LCD DISPLAY/CRT DISPLAY
6	SRAM	SELECT STATIC RAM/DYNAMIC RAM
7	MOUSE	SELECT MOUSE/LIGHT PEN

MONITOR CONTROL REGISTER

Bit 0,1 These bits select the screen vertical line number. These bits should be programmed as follows:

SCR		VERTICAL LINE NUMBER
1	0	
0	0	192
0	1	200
1	0	204
1	1	64

VERTICAL LINE SELECT (64: LCD only)

Bit 2 This bit selects the screen horizontal dot number. This should be programmed as follows:

BIT 2	HORIZONTAL DOT NUMBER
0	640 or 320
1	512 or 256

Bit 3 Selects television type between PAL/SECAM type and NTSC type, a "1" selects PAL/SECAM.

Bit 4 Selects monitor, which can be connected to this controller output, between Color Monitor and IBM PC Monochrome Monitor (The Sync signals are specialized to meet its monitor specification). The Color Monitor means normal frequency display.

Bit 5 Selects between LCD Display and CRT Display, a "1" selects LCD Display.

Bit 6 Selects RAM, which can be configurated with this controller between static RAM and dynamic RAM. A "1" selects static RAM use.

Bit 7 Selects pointing device, which can be connected directly to this controller, between Mouse and Light Pen, a "1" selects Mouse device.

This register is preset to hex "01" by the RESET signal.

5. MONO/LCD Control Register

This is an 8 bit write-only register. Its address is hex "66" within the Register Bank.

The following is a description of the MONO/LCD Control Register.

BIT	NAME	FUNCTION
0	RAJ 0	Select Raster Adjust Number of Vertical
1	RAJ 1	Display Position for LCD Upper Half
2	LS 0	Select LCD Drive Type
3	LS 1	
4	LS 2	Select LCD Drive Shift Clock
5	LS 3	
6	MON 0	Disable Gray Scale Modification
7	MON 1	Select Monochrome Adapter Visibility

MONO/LCD CONTROL REGISTER

Bit 0,1 These bits select Raster Adjust Number of vertical display position for LCD upper half. These two bits should be programmed as follows:

BIT		RASTER ADJUST NUMBER
1	0	
0	0	0
0	1	2
1	0	4
1	1	6

RASTER ADJUST NUMBER

Bit 2,3 These bits select LCD Driver Type as follows:

LS1	LS0	LCD Driver Type
0	0	Type 1 (dual one bit serial)
0	1	Type 2 (dual four bit parallel)
1	X	Type 3 (dual four bit intensity)

SELECT LCD DRIVER TYPE

Bit 4,5 These bits select LCD Driver shift clock frequency and are called LS3, 2. LS2 bit should be set "1" when 320 or 256 dot device is used. LS3 bit should be set "1" when the high speed driver are used. This frequency is divided by four when the type 2 driver interface is used.

Type 2	LS3	LS2	LCD Driver Shift Clock
0	0	0	2.685 MHz
0	0	1	1.34 MHz
0	1	0	5.37 MHz
0	1	1	2.68 MHz
1	0	0	0.67 MHz
1	0	1	0.34 MHz
1	1	0	1.34 MHz
1	1	1	0.67 MHz

SELECT LCD DRIVER SHIFT CLOCK

Bit 6 This bit, when set, disables gray scale modification and the Intensity signal to output three ("1", "0.5" or "0") levels.
The "DB" and "DI" signals should be used for the IBM PC Monochrome Monitor. This bit, when reset, enables 16 colors display.

Bit 7 This bit, when set, selects the monochrome adapter visibility. Bit 3 of the status Register indicates the video dot information, bit 0 of the status register indicates the Horizontal Sync, and the underline function becomes available. When this bit reset, the software visibility becomes the color adapter specification.

Bit 6,7 are cleared by the RESET Signal.

6. Configuration Mode Register
This is an 8 bit write-only register. Its address is hex "67" within the Register Bank.

The following is a description of the configuration Mode Register.

BIT	NAME	FUNCTION
0	EH 0	E-Clk/W-Clk for LCD
∫	∫	or
4	EH 4	Horizontal Display Position
5	M-SEL	Select M Signal (A.C. Driving Control)
6	PAGE	Enable Page Mode
7	16 bit	Enable 16 Bit CPU

CONFIGURATION MODE REGISTER

Bit 0~4 These bits value is used to divide counter to generate E-CLK (Enable Clock) or W-CLK (Weight Clock) for LCD Driver when LCD mode, or is used to adjust horizontal display position between – 7 dot to 8 dot range when CRT mode.

Bit 5 Selects the type of LCD A.C. Driving control signal period between a half of horizontal sync and vertical sync.

Bit 6 This bit, when set, enables the Page Mode function and become available to use 64K bit dynamic RAMs. The 64K byte space is divided into four display pages and is used as a multi-page display buffer.

Bit 7 This bit, when set, enables the 16 bit CPU Bus operation and the 16 bit Bus microprocessor can become host processor.

This register is cleared by the RESET signal.

7. Sprite Color Select Register
This is an 8 bit write-only register. Its address is hex "68" within the Register Bank.

The following is a description of the Sprite Color Select Register functions.

BIT	NAME	FUNCTION
0	S1-B	BLUE SPRITE 1 COLOR SELECT
1	S1-G	GREEN SPRITE 1 COLOR SELECT
2	S1-R	RED SPRITE 1 COLOR SELECT
3	S1-I	INTENSITY SPRITE 1 COLOR SELECT
4	S2-B	BLUE SPRITE 2 COLOR SELECT
5	S2-G	GREEN SPRITE 2 COLOR SELECT
6	S2-R	RED SPRITE 2 COLOR SELECT
7	S2-I	INTENSITY SPRITE 2 COLOR SELECT

SPRITE CONTROL/COLOR SELECT REGISTER

Bit 0 ~ 3 Select the Sprite 1 ANDing Foreground Color.

Bit 4 ~ 7 Select the Sprite 2 EXORing Foreground Color.

8. Control Data Register
The data, which are written in this register, are output in the RD bus on the VSY/FLML rise timing. It is possible to latch this data into the outside register and is available to use control signal or data.

9. Color Palette
The LCDC contains a 16-word by 9-bit palette in the Register Bank which takes pixel information from video RAM and uses it to select the color to display. This palette is used in all display modes.

This is write-only register and is writable anytime without any display flicker.

This palette looks like read-only memory with pixel information 4-bit addressing, which is the logical color code and is called I, R, G and B bit by software, and outputs 9-bit color data and 3-bit for each R, G, B information. This output is converted to linear R, G, B signal corresponding to the binary value by digital to analog converter. Then, 16 colors out of 512 different colors can be displayed on the screen by this color palette.

This color palette is preset by the "RESET" signal to display the same colors as the IBM PC.

10. Preset

Upon RESET. The same color scheme as the IBM PC is preset.

Using three bits apiece for R, G, and B, 512 colors are possible. Of those 256 colors, 16 colors may be saved in the color palette. Bits I, R, G, and B have meanings in IBM PC mode, however, generally the color palette selection signals do not have meaning.

I	R	G	B		R2	R1	R0	G2	G1	G0	B2	B1	B0
0	0	0	0	Black	0	0	0	0	0	0	0	0	0
0	0	0	1	Blue	0	0	0	0	0	0	1	0	0
0	0	1	0	Green	0	0	0	1	0	0	0	0	0
0	0	1	1	Cyan	0	0	0	1	0	0	1	0	0
0	1	0	0	Red	0	1	1	0	0	0	0	0	0
0	1	0	1	Magenta	1	0	0	0	0	0	1	0	0
0	1	1	0	Brown	1	0	0	0	1	1	0	0	0
0	1	1	1	White	1	0	0	1	0	0	1	0	0
1	0	0	0	Gray	0	0	1	0	0	1	0	0	1
1	0	0	1	Light Blue	0	0	0	0	0	0	1	1	0
1	0	1	0	Light Green	0	0	0	1	1	0	0	0	0
1	0	1	1	Light Cyan	0	0	0	1	1	0	1	1	0
1	1	0	0	Light Red	1	0	1	0	0	0	0	0	0
1	1	0	1	Light Magenta	1	1	0	0	0	0	1	1	0
1	1	1	0	Yellow	1	1	0	1	1	0	0	0	0
1	1	1	1	White (High Intensity)	1	1	1	1	1	1	1	1	1

3DFH (Display Page REGISTER)

This is a 3 bit write-only register. It can't be read and its address is hex "3DFH" of the four least significant bits of the I/O address with a "0" ★IOSEL signal.

When the Page Mode is enabled, this register selects a page from four 16KB display pages in a 64K bytes space. The Page Mode is not supported on the static RAM system configuration due to pin number limit, but it becomes available for use adding by external circuits.

Other registers function are as same as 6845 registers.

FLOPPY DISK CONTROLLER

Address	Bit	Bit data	Description
3F2H	0,1	00 01 10 11	Drive select A Drive select B Drive select C Drive select D
	2	0	The FDC is held reset when this bit is clear. It must be set by the program to enable the FDC.
	3	0/1	Disable Enable INT & DMA Request
	4	0/1	Drive A Motor OFF/ON & In-use
	5	0/1	Drive B Motor OFF/ON & In-use
	6	0/1	Drive C Motor OFF/ON & In-use
	7	0/1	Drive D Motor OFF/ON & In-use
3F4H	0 ~ 7	0/1	FDC Mais Status Register
3F5H	0 ~ 7	0/1	FDC Data Register

Main Status Register

No.	Pin Name	Function
DB_0	D_0B (FDD 0 Busy)	FDD number 0 is in the seek mode. If any of the DnB bits is set FDC will not accept read or write command.
DB_1	D_1B (FDD 1 Busy)	FDD number 1 is in the seek mode. If any of the DnB bits is set FDC will not accept read or write command.
DB_2	D_2B (FDD 2 Busy)	FDD number 2 is in the seek mode. If any of the DnB bits is set FDC will not accept read or write command.
DB_3	D_3B (FDD 3 Busy)	FDD number 3 is in the seek mode. If any of the DnB bits is set FDC will not accept read or write command.
DB_4	DB (FDC Busy)	A Read or Write command is in process. FDC will not accept any other command.
DB_5	EXM (Execution Mode)	This bit is set only during execution phase in non-DMA mode. When DB_5 goes low, execution phase has ended and result phase has started. It operates only during non-DMA mode of operation.
DB_6	DIO (Data Input/ Output)	Indicates direction of data transfer between FDC and data register. If DIO=1, then transfer is from data register to the processor. If DIO=0, then transfer is from the processor to data register.
DB_7	RQM (Request for Master)	Indicates data register is ready to send or receive data to or from the processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

Status Register Identification

Pin No.	Name	Function
Status Register 0		
D_7, D_6	IC (Interrupt Code)	D_7=0 and D_6=0 Normal termination of command, (NT). Command was completed and properly executed.
		D_7=0 and D_6=1 Abnormal termination of command, (AT). Execution of command was started but was not successfully completed.
		D_7=1 and D_6=0 Invalid command issue, (IC). Command which was issued was never started.
		D_7=1 and D_6=1 Abnormal termination because during command execution the ready signal from FDD changed state.
D_5	SE (Seek End)	When the FDC completes the Seek command, this flag is set to 1 (high).
D_4	EC (Equipment Check)	If a fault signal is received from the FDD, or if the track 0 signal falls to occur after 77 step pulses (Recalibrate Command) then this flag is set.
D_3	NR (Not Ready)	When the FDD is in the not-ready state and a Read or Write command is issued, this flag is set. If a Read or Write command is issued to side 1 of a single-sided drive, then this flag is set.
D_2	HD (Head Address)	This flag is used to indicate the state of the head at interrupt.
D_1	US_1 (Unit Select 1)	This flag is used to indicate a drive unit number at interrupt.
D_0	US_0 (Unit Select 0)	This flag is used to indicate a drive unit number at interrupt.

Pin No.	Name	Function
Status Register 1		
D_7	EN (End of Cylinder)	When the FDC tries to access a sector beyond the final sector of a cylinder, this flag is set.
D_6		Not used. This bit is always 0 (low).
D_5	DE (Data Error)	When the FDC detects a CRC(1) error in either the ID field or the data field, this flag is set.
D_4	OR (Overrun)	If the FDC is not serviced by the host system during data transfers within a certain time interval, this flag is set.
D_3		Not used. This bit is always 0 (low).
D_2	ND (No Data)	During execution of Read Data. Write Deleted Data or Scan command, if the FDC cannot find the sector specified in the IDR(2) Register, this flag is set.
		During execution of the Read ID command, if the FDC cannot read the ID field without an error, then this flag is set.
		During execution of the Read A Cylinder command, if the starting sector cannot be found, then this flag is set.
D_1	NW (Not Writable)	During execution of Write Data, Write Deleted Data or Format A Cylinder command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	MA (Missing Address Mark)	If the FDC cannot detect the data address mark or deleted data address mark, this flag is set. Also at the same time, the MD (missing address mark in data field) of status register 2 is set.

Pin No.	Name	Function
Status Register 2		
D_7		Not used. This bit is always 0 (low).
D_6	CM (Control Mark)	During execution of the Read Data or Scan command, if the FDC encounters a sector which contains a deleted data address mark, this flag is set.
D_5	DD (Data Error in Data Field)	If the FDC detects a CRC error in the data field then this flag is set.
D_4	WC (Wrong Cylinder)	This bit is related to the ND bit, and when the contents of C(3) on the medium is different from that stored in the IDR, this flag is set.
D_3	SH (Scan Equal Hit)	During execution of the Scan command, if the condition of "equal" is satisfied, this flag is set.
D_2	SN (Scan Not Satisfied)	During execution of the Scan command, if the FDC cannot find a sector on the cylinder which meets the condition, then this flag is set.
D_1	BC (Bad Cylinder)	This bit is related to the ND bit, and when the contents of C on the medium is different from that stored in the IDR and the contents of C is FFH, then this flag is set.
D_0	MD (Missing Address Mark in Data Field)	When data is read from the medium, if the FDC cannot find a data address mark or deleted data address mark, then this flag is set.

Pin No.	Name	Function
Status Register 3		
D_7	FT (Fault)	This bit is used to indicate the status of the fault signal from the FDD.
D_6	WP (Write Protected)	This bit is used to indicate the status of the write protected signal from the FDD.
D_5	RY (Ready)	This bit is used to indicate the status of the ready signal from the FDD.
D_4	T0 (Track 0)	This bit is used to indicate the status of the track 0 signal from the FDD.
D_3	TS (Two-Side)	This bit is used to indicate the status of the two-side signal from the FDD.
D_2	HD (Head Address)	This bit is used to indicate the status of the side select signal to the FDD.
D_1	US_1 (Unit Select 1)	This bit is used to indicate the status of the unit select 1 signal to the FDD.
D_0	US_0 (Unit Select 0)	This bit is used to indicate the status of the unit select 0 signal to the FDD.

Notes:

(1) CRC=Cyclic Redundancy Check
(2) IDR=Internal Data Register
(3) Cylinder (C) is described more fully in the Command Symbol Description.

Command Symbpl Description

Name	Function
A_0 (Address Line 0)	A_0 controls selection of main status register ($A_0=0$) ro data register ($A_0=1$)
C (Cylinder Number)	C stands for the current/selected cylinder (track) numbers 0 through 76 of the medium.
D (Data)	D stands for the data pattern which is going to be written into a sector.
D_7 – D_0 (Data Bus)	8-bit data bus, where D_7 stands for a most significant bit, and D_0 stands for a least signification bit.
DTL (Data Length)	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT (End of Track)	EOT stands for the final sector number on a cylinder. During read or write operations, FDC will stop data transfer after a sector number equal to EOT.
GPL (Gap Length)	GPL stands for the length of gap 3. During Read/Write commands this value determines the number of bytes that VC0 sync will stay low after two CRC bytes. During Format command it determines the size of gap 3.
H (Head Address)	H stands for head number 0 or 1, as specified in ID field.
HD (Head)	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H=HD in all command words.)
HLT (Head Load Tim(	HLT stands for the head load time in .he FDD (2 to 254 ms in 2 ms increments).
HUT (Head Unload Time)	HUT stands for the head unload time after a Read or Write operation has occurred (16 to 240 ms in 16 ms increments).
MF (FM or MFM Mode)	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT (Multitrack)	If MT is high, a multitrack operation is performed. If MT=1 after finishing read/write operation on side 0, FDC will automatically start searching for sector 1 on side 1.

Name	Function
N (Number)	N stands for the number of data bytes written in a sector.
NCN (New Cylinder Number)	NCN stands for a new cylinder number which is going to be reached as a result of the seek operation; desired position of head.
ND (Non-DMA Mode)	ND stands for operation in the non-DMA mode.
PCN (Present Cylinder Number)	PCN stands for the cylinder number at the completion of Sense Interrupt Status command, position of head at present time.
R (Record)	R stands for the sector number which will be read or written.
R/W (Read/Write)	R/W stands for either Read (R) or Write (W) signal.
SC (Sector)	SC indicates the number of sectors per cylinder.
SK (Skip)	SK stands for skip deleted data address mark.
SRT (Step Rate Time)	SRT stands for the stepping rate for the FDD (1 to 16 ms in 1 ms increments). Stepping rate applies to all drives (FH=1ms, EH=2ms, etc.)
ST0 – ST3 (Status 0 – 3)	ST0 – ST3 stands for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0=0$). ST0 – ST3 may be read only after a command has been executed and contains information relevant to that particular command.
STP	During a scan operation, if STP=1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP=2, then alternate sectors are read and compared.
US_0, US_1 (Unit Select)	US stands for a selected drive number 0 or 1.

Instruction Set (1)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read Data										
Command	W	MT	MF	SK	0	0	1	1	0	Command codes
	W	X	X	X	X	X	HD	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The 4
	W	←			H				→	bytes are compared against header on floppy disk.
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Excution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

Note:

(1) In the Instruction Code, X=don't care (usually set to 0).

(2) A_0 should be 0 for SET STANDBY, RESET STANDBY, and SOFTWARE RESET commands and 1 for all other commands.

Instruction Set (2)

Phase	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Remarks
Read Deleted Data										
Command	W	MT	MF	SK	0	1	1	0	0	Command codes
	W	X	X	X	X	X	HD	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The 4
	W	←			H				→	bytes are compared against header on floppy disk.
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Write Data										
Command	W	MT	MF	0	0	0	1	0	1	Command codes
	W	X	X	X	X	X	HD	US1	US0	
	W	←			C				→	Sector ID information prior to command execution. The 4
	W	←			H				→	bytes are compared against header on floppy disk.
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Write Deleted Data										
Command	W	MT	MF	0	0	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution. The 4
	W	←			H				→	bytes are compared against header on floppy disk.
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			DTL				→	
Execution										Data transfer between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Scan Low or Equal										
Command	W	MT	MF	SK	1	1	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

Instruction Set (3)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Scan High or Equal										
Command	W	MT	MF	SK	1	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Execution										Data compared between the FDD and main system
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Recalibrate										
Command	W	0	0	0	0	0	1	1	1	Command codes
	W	X	X	X	X	X	0	US_1	US_0	
Execution										Head retracted to track 0
Sense Interrupt Status										
Command	W	0	0	0	0	1	0	0	0	Command codes
Result	R	←			ST0				→	Status information about the FDC at the end of seek operation
	R	←			PCN				→	
Specify										
Command	W	0	0	0	0	0	0	1	1	Command codes
	W	←	SRT	→	←		HUT		→	
	W	←		HLT					ND	
Sense Drive Status										
Command	W	0	0	0	0	0	1	0	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Result	R	←			ST3				→	Status informatin about FDD
Seek										
Command	W	0	0	0	0	1	1	1	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			NCN				→	
Execution										Head is positioned over proper cylinder on diskette
Invalid										
Command	W	←			Invalid Codes				→	Invalid Command codes (No op – FDC goes into standby state)
Result	R	←			ST0				→	ST0=80H
Set Standby										
Command	W	0	0	1	1	0	1	0	1	Command codes
Execution										Enter standby mode
Reset Standby										
Command	W	0	0	1	1	0	1	0	0	Command codes
Execution										Disable standby mode
Software Reset										
Command	W	0	0	1	1	0	1	1	0	Command codes
Execution										Same as hardware reset

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read a Track										
Command	W	0	MF	SK	0	0	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←				C			→	Sector ID information prior to command execution.
	W	←				H			→	
	W	←				R			→	
	W	←				N			→	
	W	←				EOT			→	
	W	←				GPL			→	
	W	←				DTL			→	
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	←				ST0			→	Status information after command execution
	R	←				ST1			→	
	R	←				ST2			→	
	R	←				C			→	Sector ID information after command execution
	R	←				H			→	
	R	←				R			→	
	R	←				N			→	

Instruction Set (4)

Phase	R/W	Instruction Code D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Remarks
Read ID										
Command	W	0	MF	0	0	1	0	1	0	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
Execution										The first correct ID information on the cylinder is stored in data register.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information read during excecution phase from floppy disk.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Format a Track										
Command	W	0	MF	0	0	1	1	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			N				→	Bytes/sector
	W	←			SC				→	Sectors/track
	W	←			GPL				→	Gap 3
	W	←			D				→	Filter byte
Execution										FDC formats an entire track.
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	In this case, the ID information has no meaning
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	
Scan Equal										
Command	W	MT	MF	SK	1	0	0	0	1	Command codes
	W	X	X	X	X	X	HD	US_1	US_0	
	W	←			C				→	Sector ID information prior to command execution.
	W	←			H				→	
	W	←			R				→	
	W	←			N				→	
	W	←			EOT				→	
	W	←			GPL				→	
	W	←			STP				→	
Result	R	←			ST0				→	Status information after command execution
	R	←			ST1				→	
	R	←			ST2				→	
	R	←			C				→	Sector ID information after command execution.
	R	←			H				→	
	R	←			R				→	
	R	←			N				→	

COM1 CONTROL

The UART includes ten registers. The user can access and control any of the UART register via the CPU. These registers are used to control the operations of the UART and to transmit and receive data.

Internal Registers

	Address	Register/ Buffer Name	Data Bit Number							
			7	6	5	4	3	2	1	0
3F8H	0 (DLAB=0)	Receiver Data Buffer (RDB)	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
3F8H	0 (DLAB=0)	Transmitter Data Buffer (TDB)	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0
3F9H	1 (DLAB=0)	Interrupt Enable Register (IER)	—	—	—	—	EMSI	ELSI	ETDB-EI	ERDRI
3FAH	2	Interrupt Ident. Register (IIR)	—	—	—	—	—	IID1	IID0	INTF
3FBH	3	Line Control Register (LCR)	DLAB	SBRK	STCP	EPS	PEN	STB	WLS1	WLS0
3FCH	4	MODEM Control Register (MCR)	—	—	—	LOOP	OUT2	OUT1	RTS	DTR
3FDH	5	Line Status Register (LSR)	—	TEMP	TDBE	BD	FE	PE	OE	RDR
3FEH	6	MODEM Status Register (MSR)	DCD	CI	DSR	CTS	DDCD	TECI	DDSR	DCTS
3FFH	7	Scratchpad Register (SCR)	D7	D6	D5	D4	D3	D2	D1	D0 CS1
3F8H	0 (DLAB=1)	Divisor Latch (LS) (DLL)	B7	B6	B5	B4	B3	B2	B1	B0
3F9H	1 (DLAB=1)	Divisor Latch (MS) (DLM)	B15	B14	B13	B12	B11	B10	B9	B8

—: Always 0

Note: The RDB and IIR are read-only registers. The TDB is write-only register. Any other registers are possible to read and write, but writting to the Status Register (LSR, MSR) during the communication are not recommended as these operations are used for diagnostic testing by the interrupt and the simulation of the receiver error.

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A division of Tandy Corporation
Fort Worth, Texas 76102

3A8

Printed in Japan